

The diagram illustrates the system architecture of the Quanta Computer Q870. The central component is the **ICH9-M** (676 BGA, PG 11,12,13,14), which serves as the main interface for various components.

**Processor and Memory:** The **Penryn** (478 Micro-FCPGA, PG 3,4) is connected to the **Cantiga** (1299 uFCBGA, PG 5,6,7,8,9,10) via a 667 / 800 / 1066 MHz FSB. The **Cantiga** is connected to two **DDR2-SODIMM** modules (PG 15,16) via 667 / 800 MHz DDR II.

**Storage and Expansion:** The **ICH9-M** is connected to **SATA-ODD** (PG 36) and **SATA-HDD** (PG 36) via SATA. It also connects to **PCIEx16**, **PCIEx1**, **PCIEx2**, and **USB2.0** ports. The **ICH9-M** is connected to the **BIOS** (PG 37) via LPC.

**Power and Thermal Management:** The **POWER** section includes **REGULATOR** (+1.5V\_RUN/+1.05V\_VCCP, PG 48), **REGULATOR** (+1.8V\_SUS/+1.25V\_RUN/+0.9V\_DDR\_VTT, PG 49), **CPU VR** (PG 51), **DC/DC** (+3.3V\_ALW/+5V\_ALW/+15V\_ALW, PG 52), and **VGA Core** (PG 50). The **FAN & THERMAL** section includes **CLOCK** (SLG8SP513V (QFN-64), PG 17) and **SMSC1423** (PG 39).

**Peripherals and I/O:** The **ICH9-M** is connected to **Audio/AMP** (STAC9228/92HD73C, PG 40), **Camera + D-MIC** (PG 41), **KBC** (ITE8512, PG 31), **Keyboard** (PG 37), **Touchpad** (PG 37), **Flash 2Mbytes** (PG 32), **USER INTERFACE** (PG 38), **Biometric** (PG 38), **8-in-1 Card Reader** (R5C833, PG 28), **1394 CONN.** (PG 29), **Card Reader CONN.** (PG 30), **EXPRESS-CARD** (PG 30), **MINI-CARD WLAN** (PG 34), **MINI-CARD WWAN** (PG 33), **MINI-CARD WPAN** (PG 33), **LAN BCM5784M** (PG 42), **RJ45/Magnetics** (PG 43), **Panel Connector** (PG 26), **CRT CONN.** (PG 27), and **HDMI CONN.** (PG 25).

**Other Components:** The **ICH9-M** is connected to **ATM M86-ME-LP** (PG 18,19,20,21,22) via **PCIEx16**, **DP BUS**, and **USB2.0 x3**. The **ICH9-M** is connected to **PI3VDP411LSZDE** (PG 18) via **USB conn x 3** (PG 35).

The diagram is a detailed block diagram showing the interconnections between various components of the Quanta Computer Q870 system. The components are represented by boxes, and the connections are shown as lines. The components are organized into several groups: Power, Fan & Thermal, Processor, Memory, Storage, Peripherals, and I/O. The connections are labeled with their respective names and page numbers. The diagram is a technical drawing and is not a photograph.


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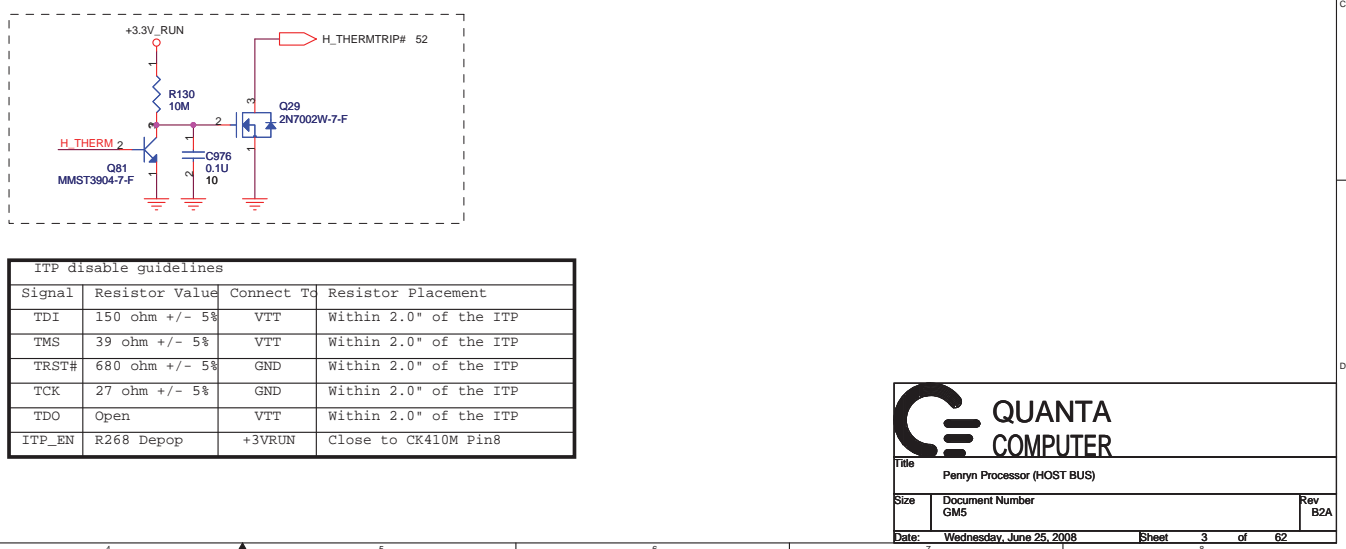
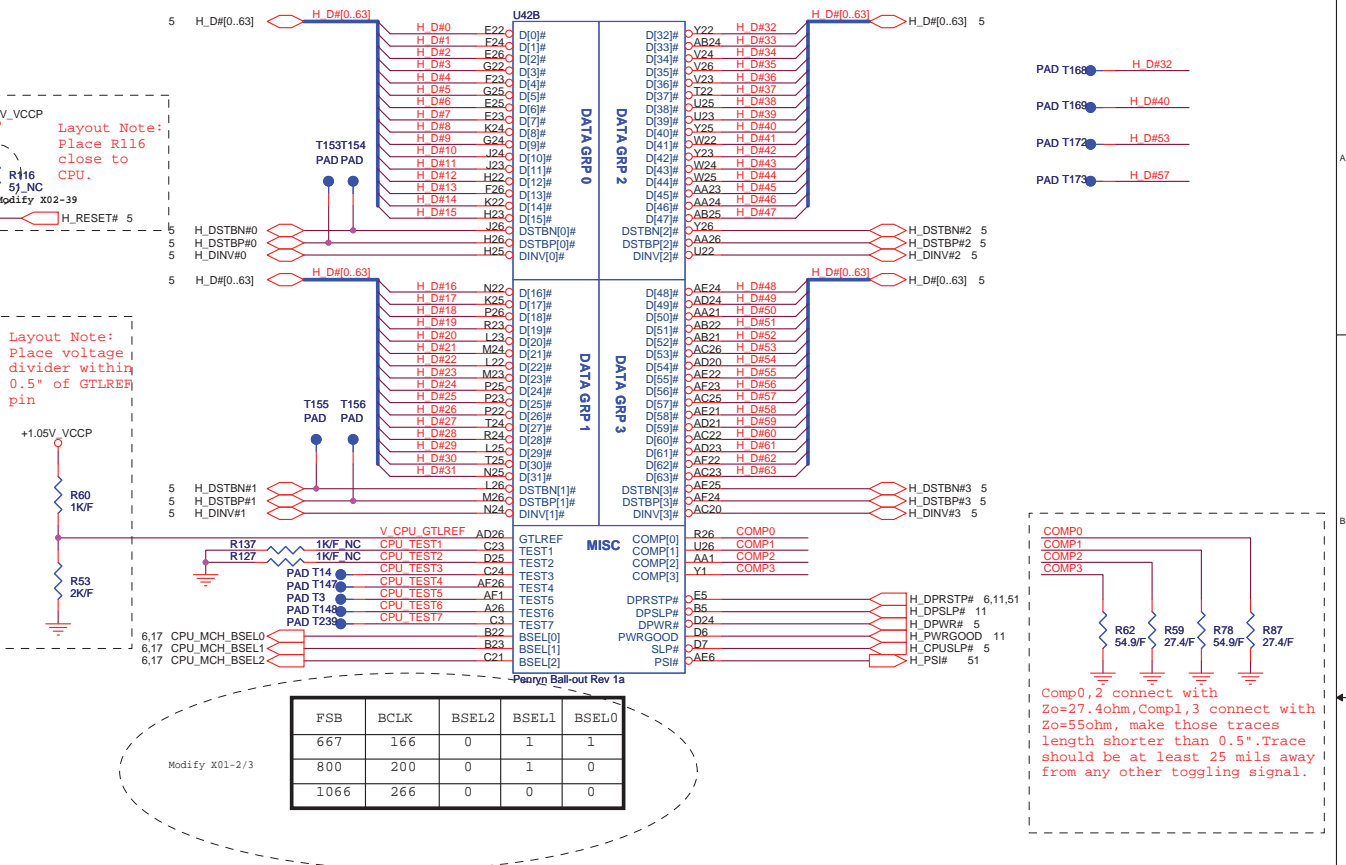
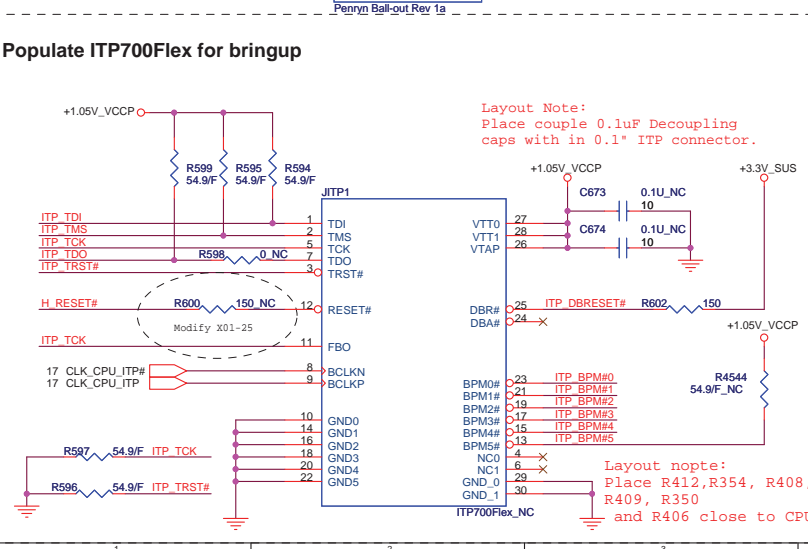
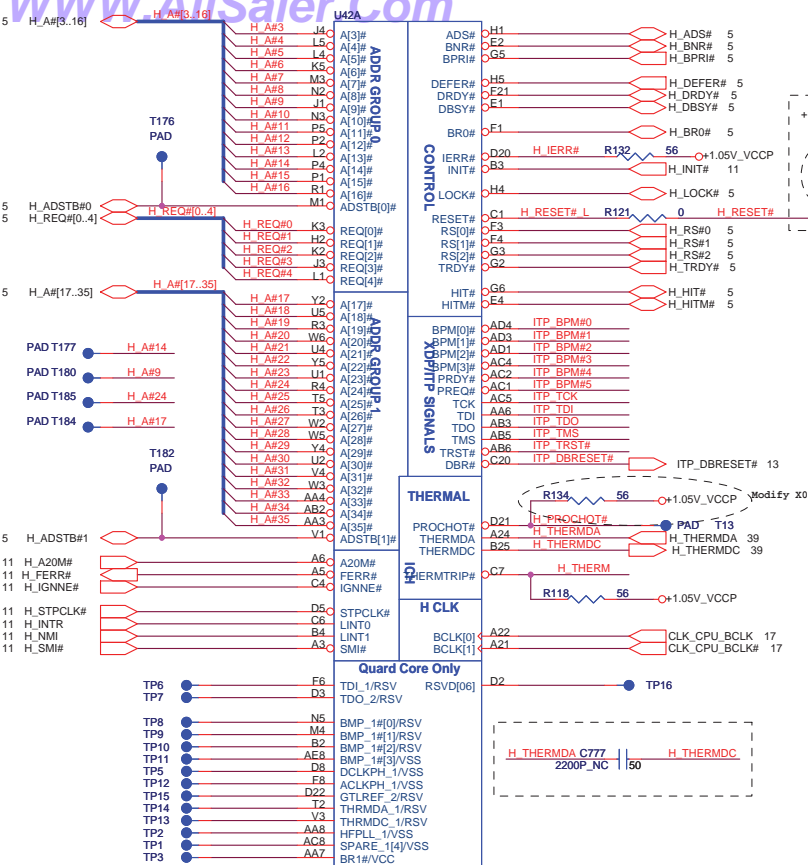
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Penryn
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26	LCD connector
27	CRT
28	Card reader PCI interface
29	Card reader & 1394
30	Express card & card reader conn.
31	SIO
32	Flash/RTC
33	WWAN/WPAN
34	WLAN
35	USB port
36	SATA HDD & ODD
37	TP/KB/MB/CIR
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39	FAN/Thermal
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42-43	Docking Conn/Q-Switch
44	System Reset Circuit
45-46	Screw hole & Charger
47	Blank page
48	1.05VCCP & 1.5VRUN
49	1.8VSUS & 0.9VTT
51	CPU_ISL6266 (2phase)
52	D/D ISL6237 3.3V/5V
53	RUN Power Switch
54	DCIN,Batt
55	EMI CAP
56	SMBUS BLOCK
57-58	Power statu & Block diagram

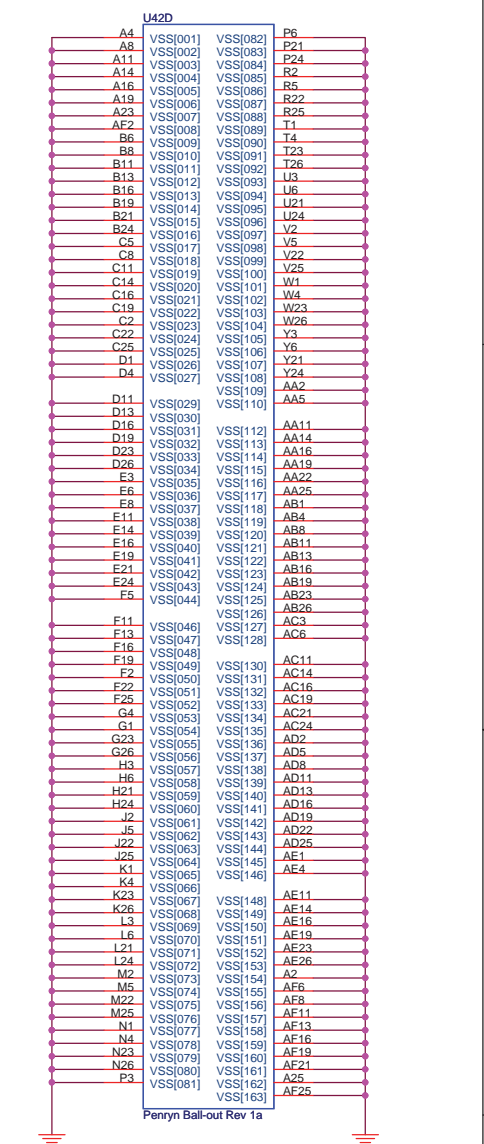
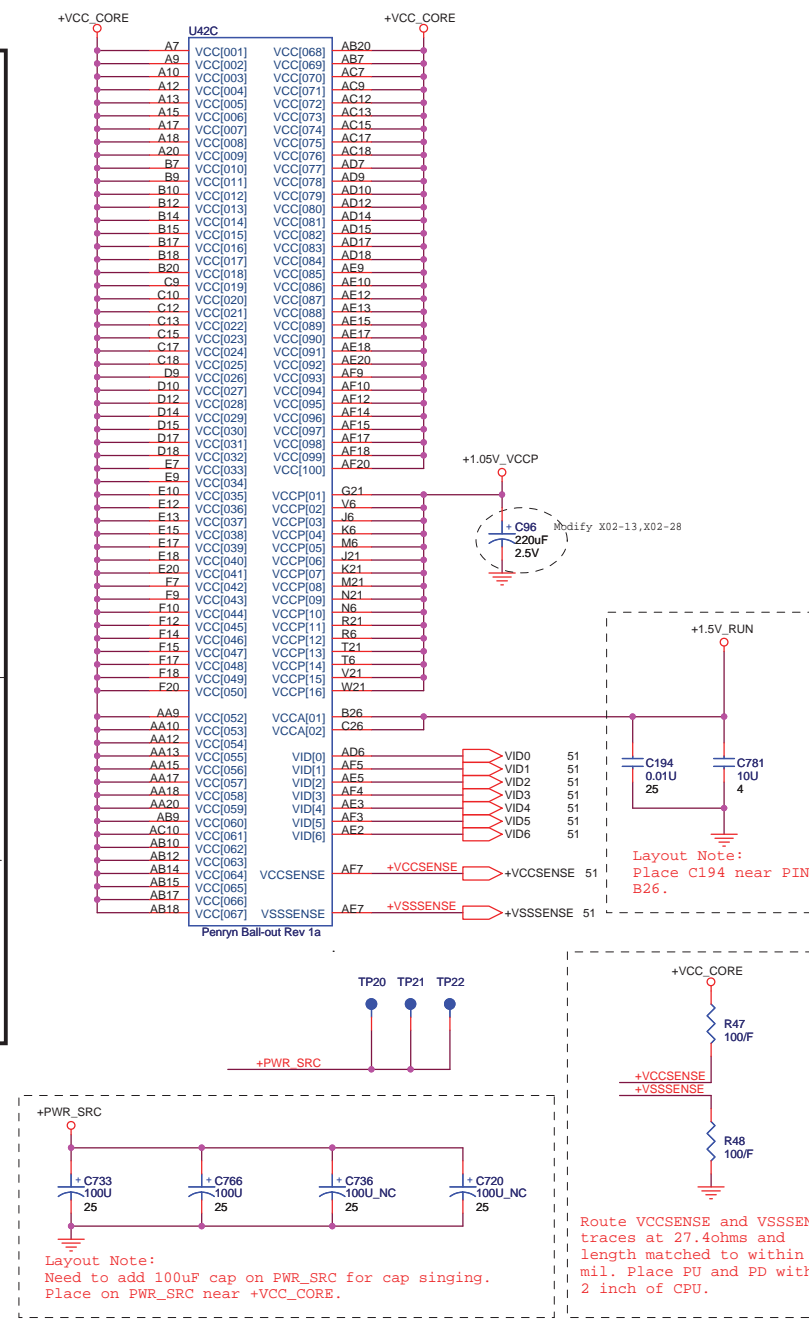
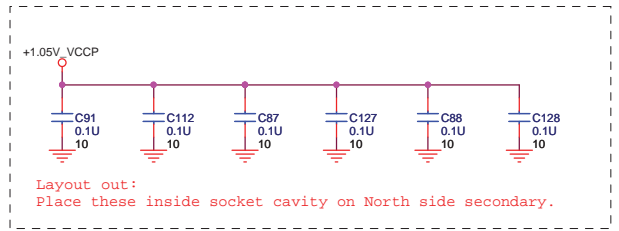
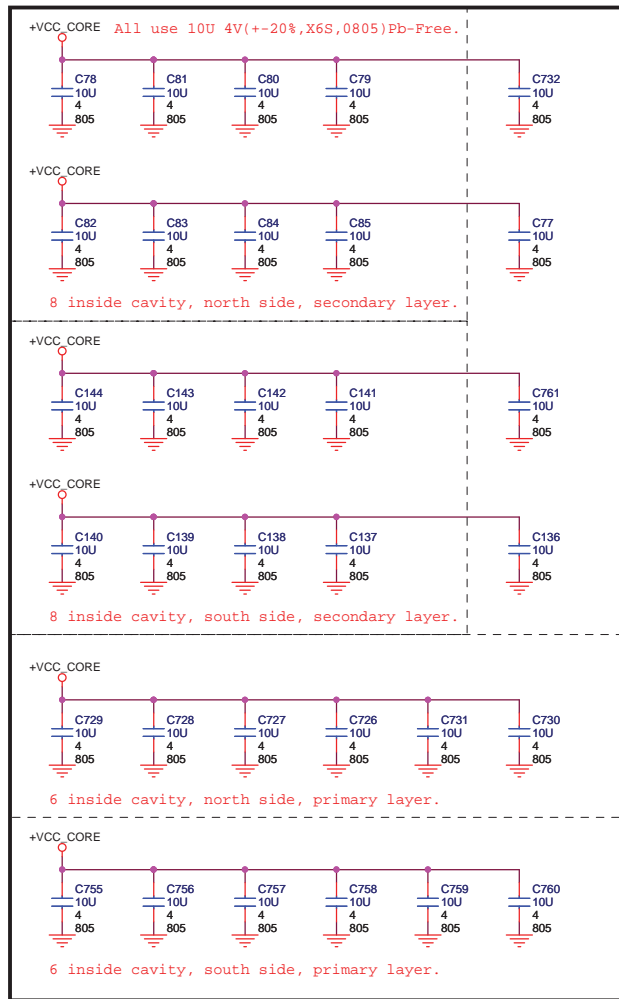
## Power States

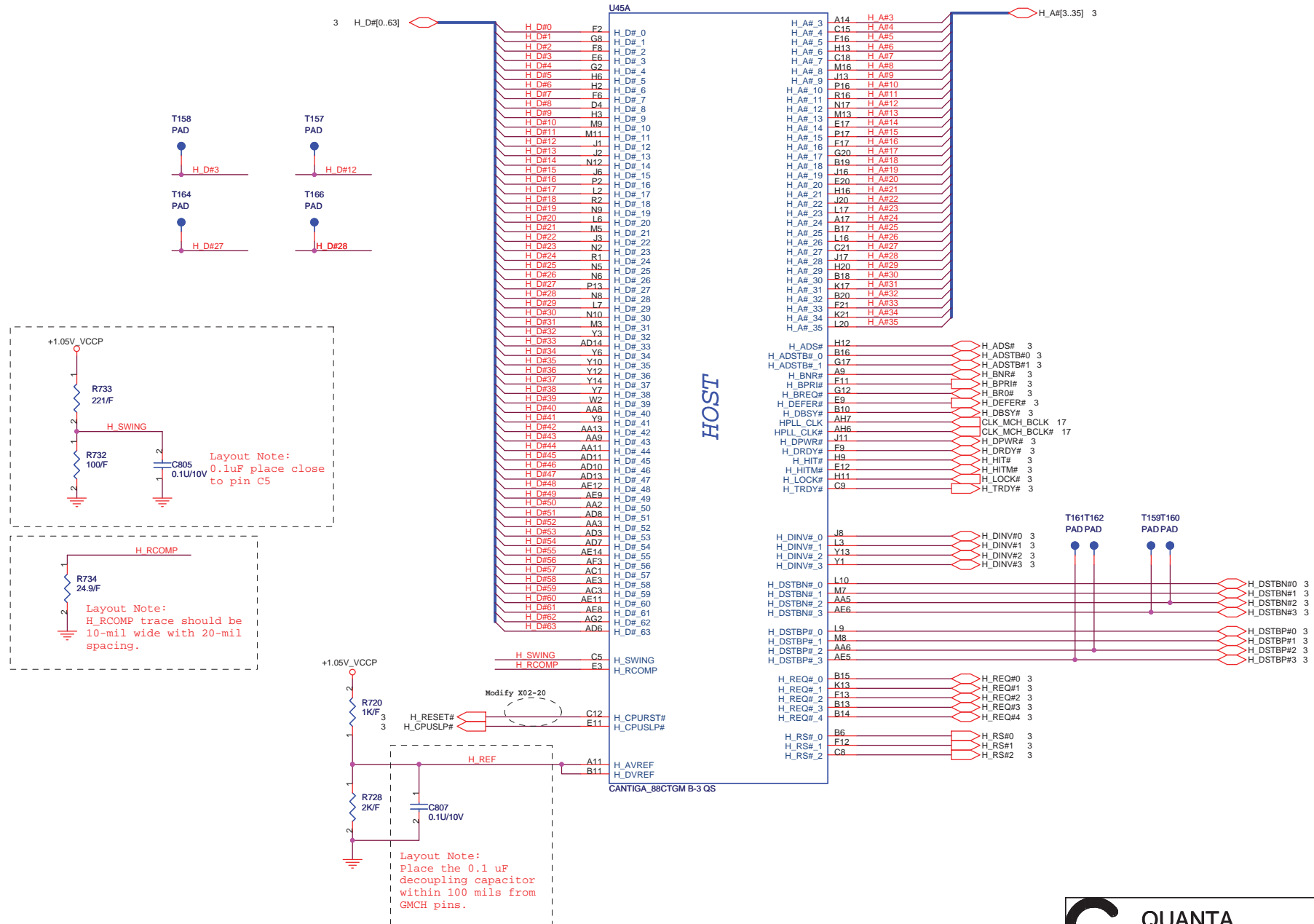
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CANTIGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CANTIGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	

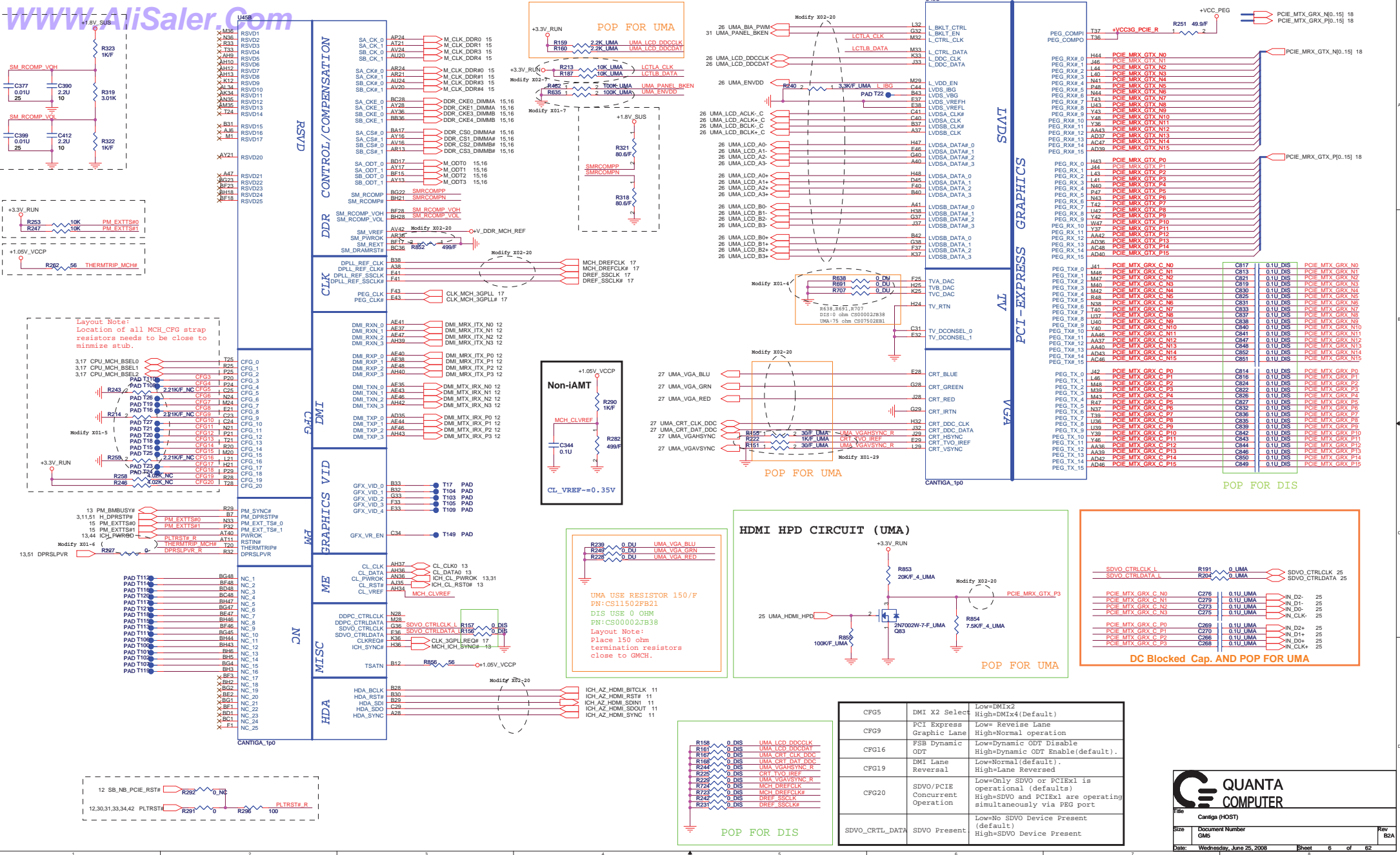
 QUANTA COMPUTER		
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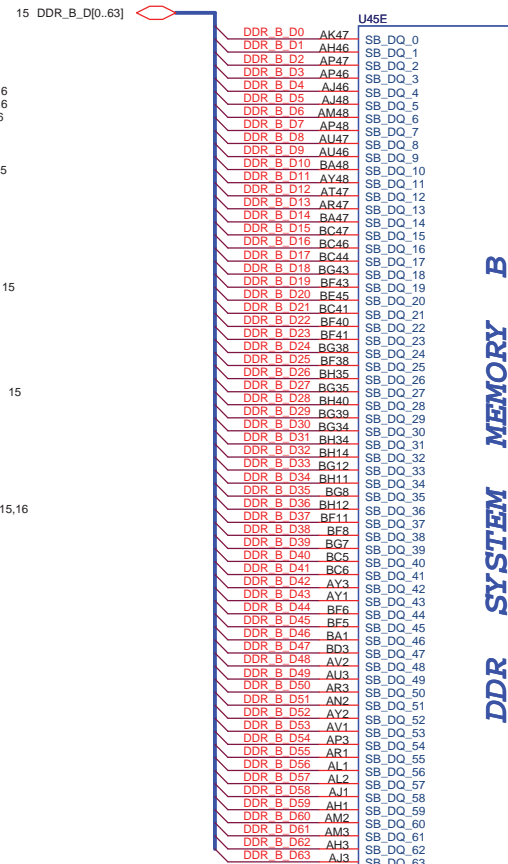
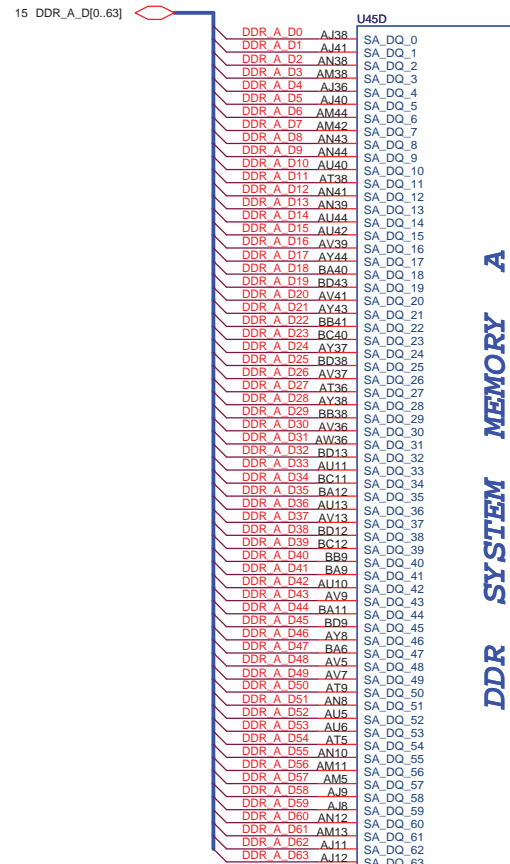
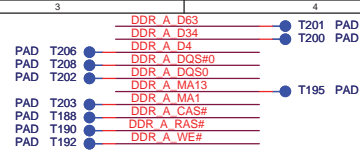






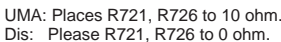




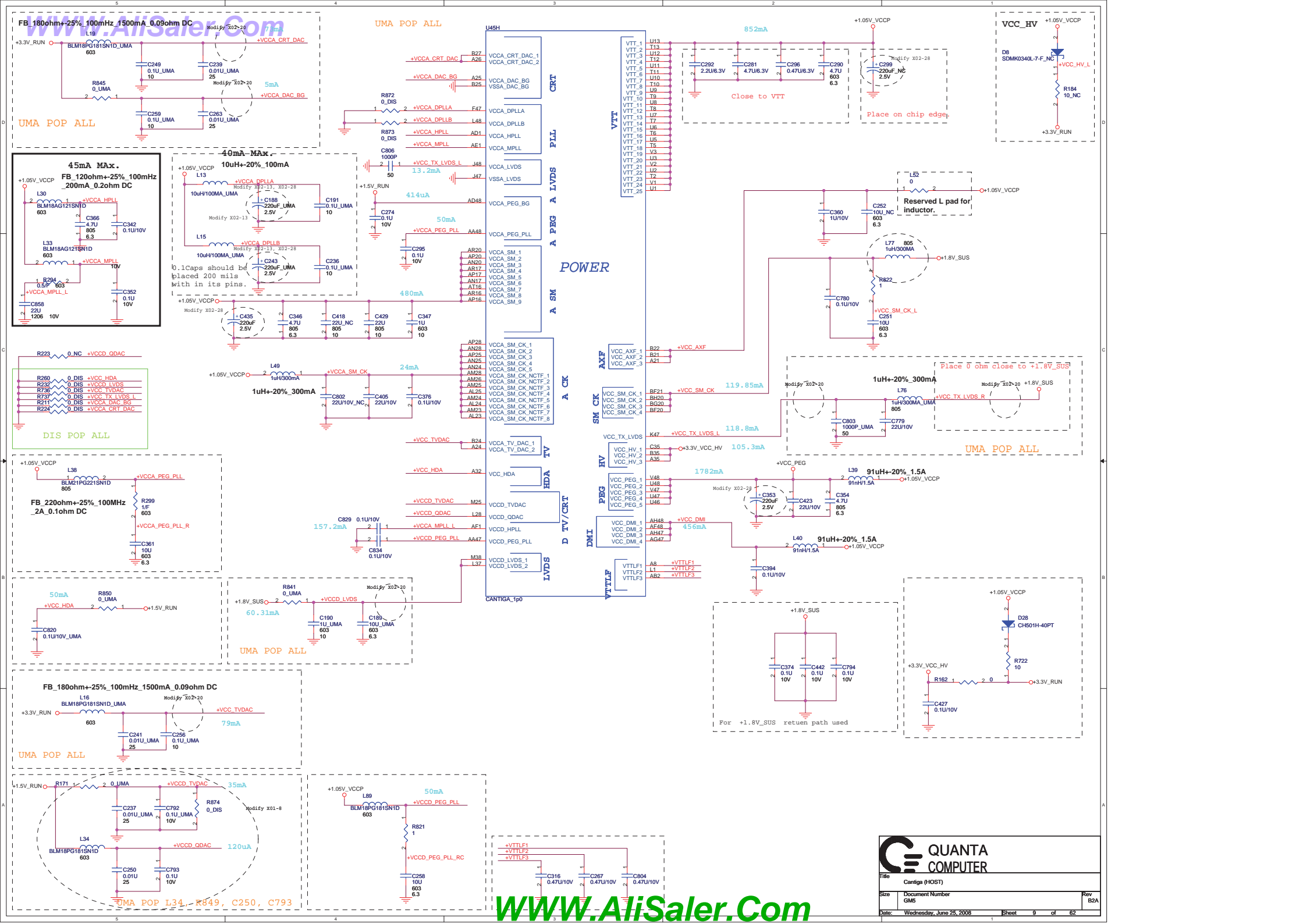


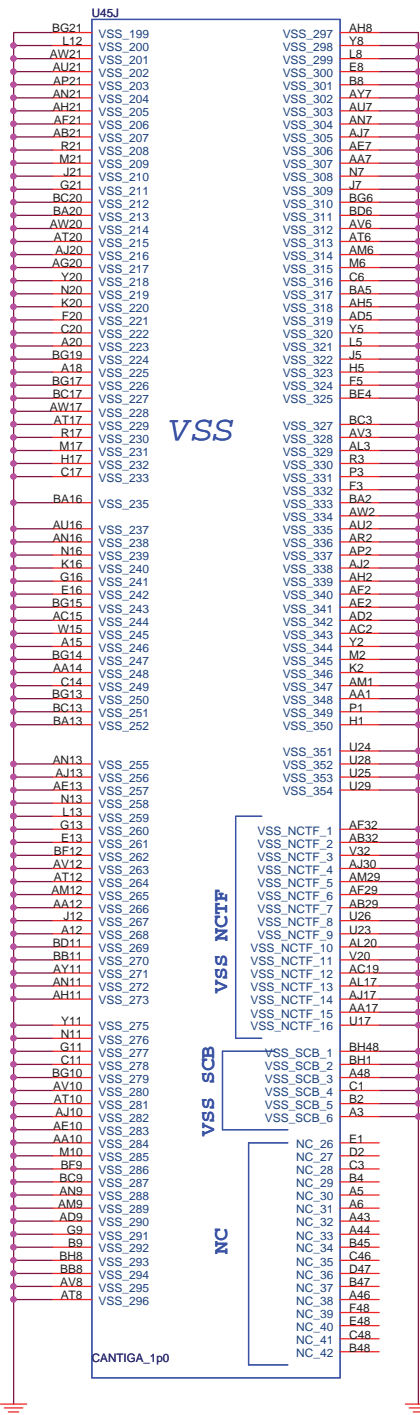
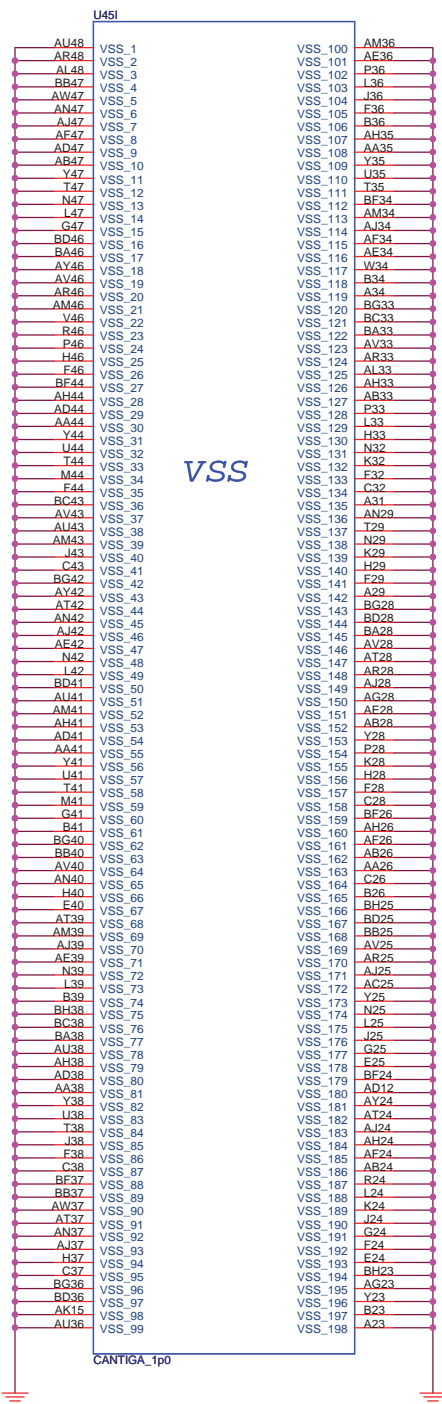
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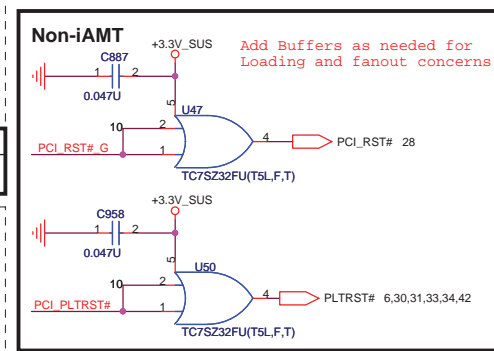
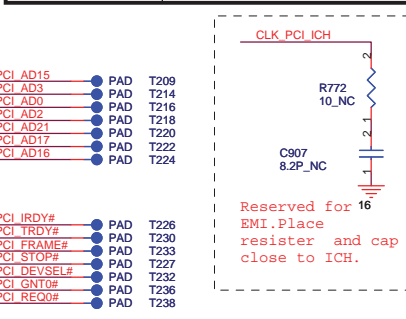
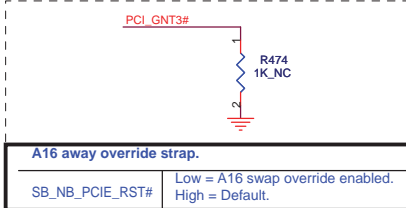
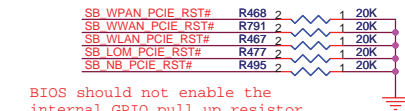
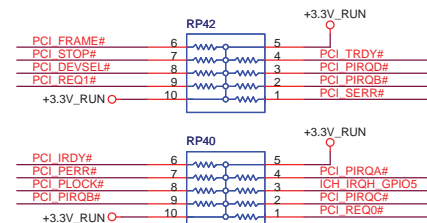
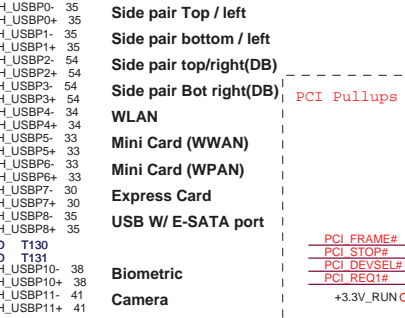
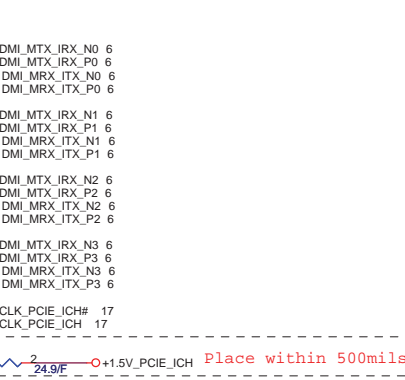
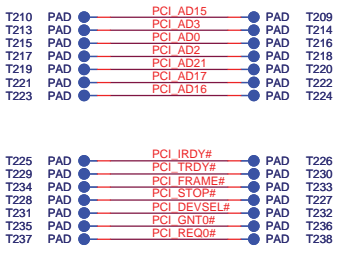
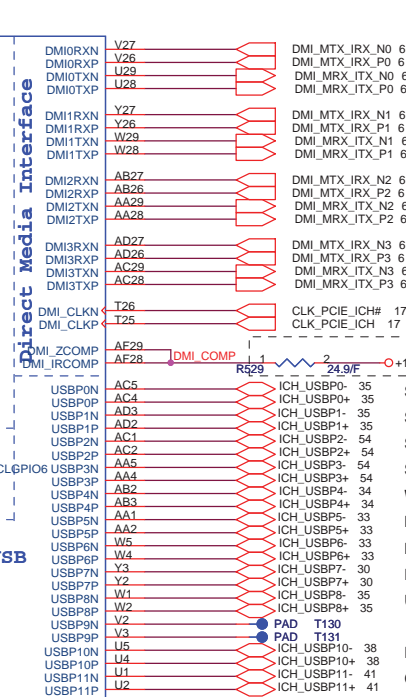
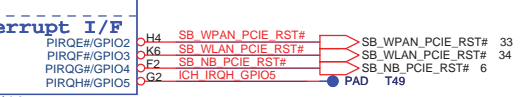
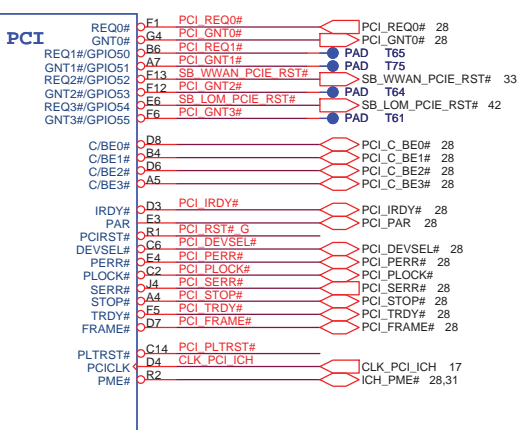
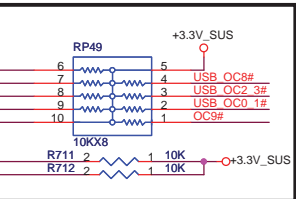
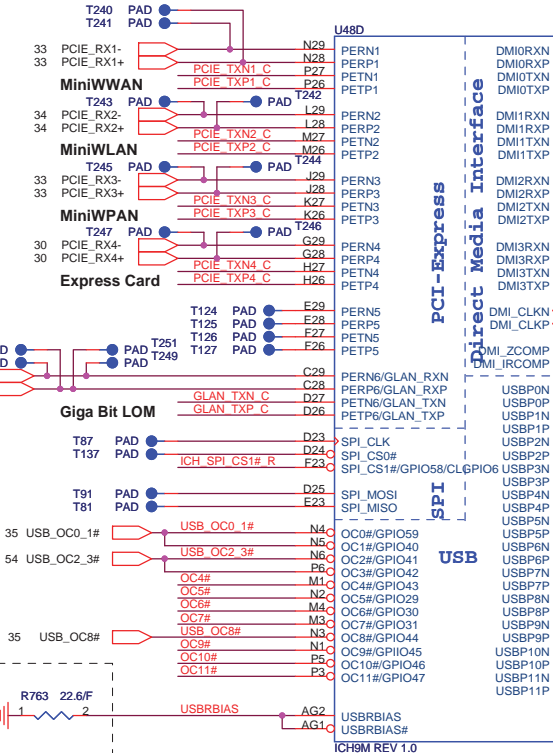
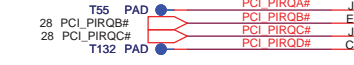
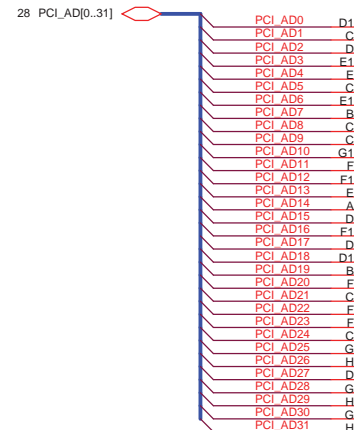
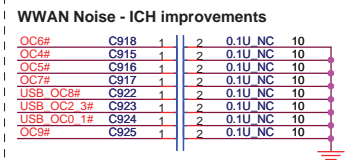
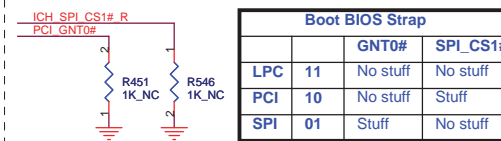
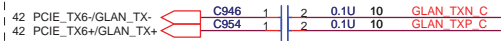




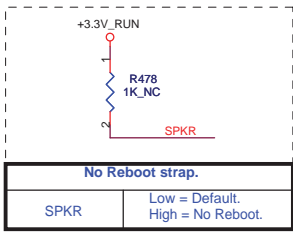
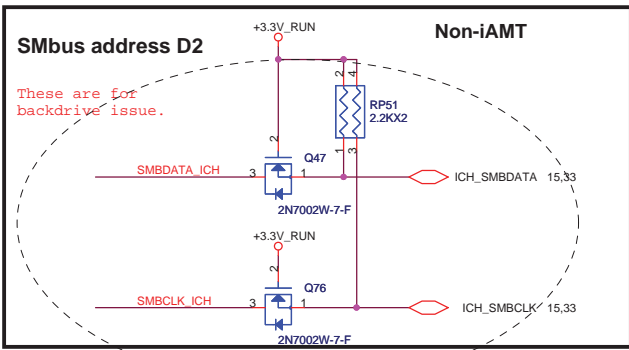
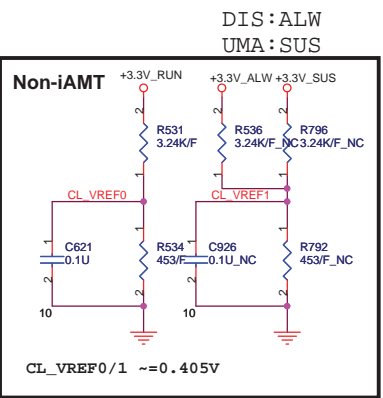
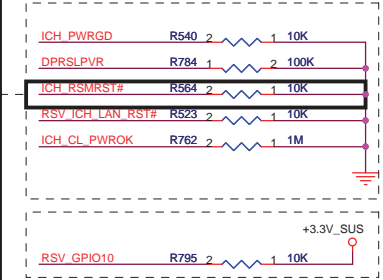
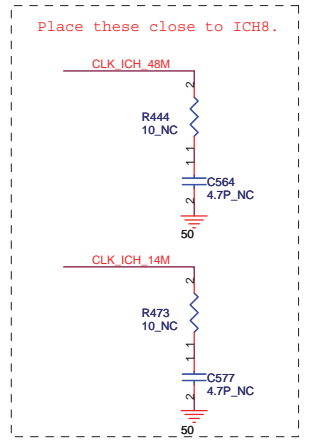
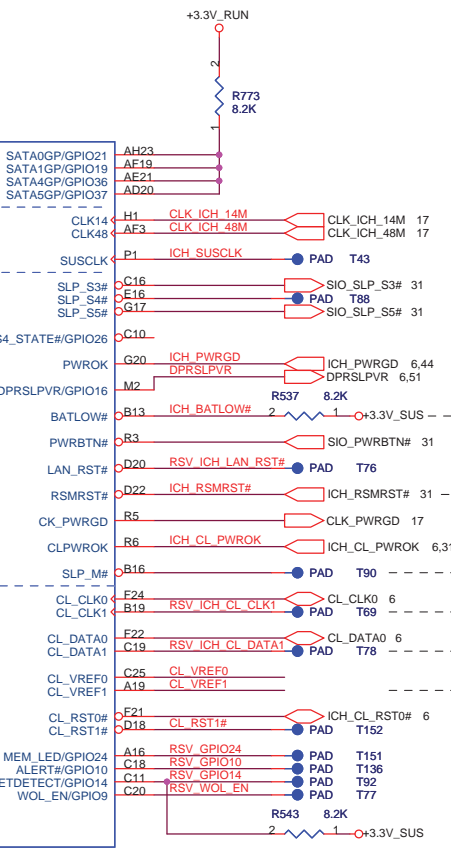
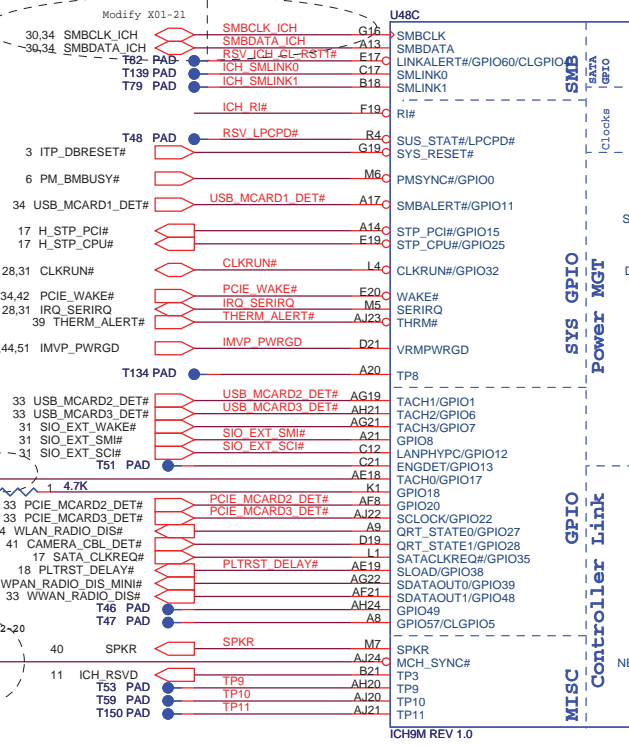
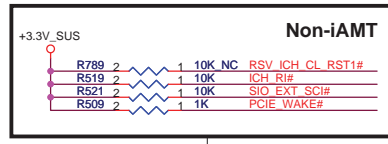
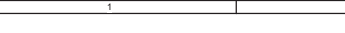
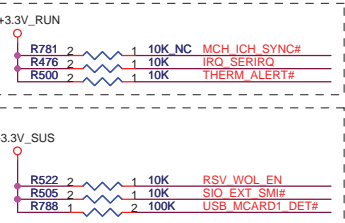
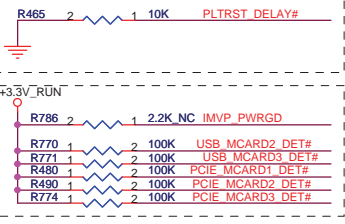
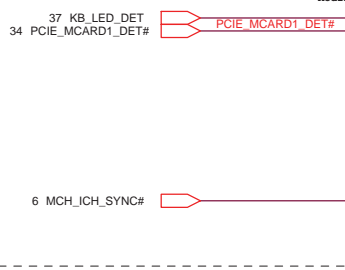
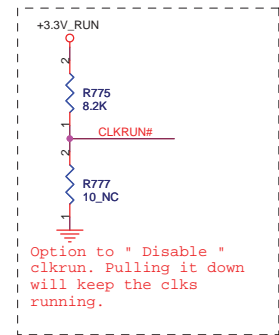
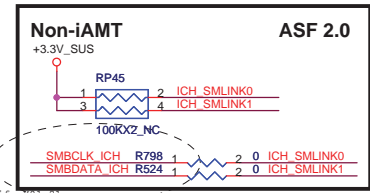
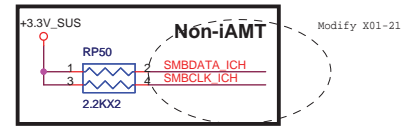


		
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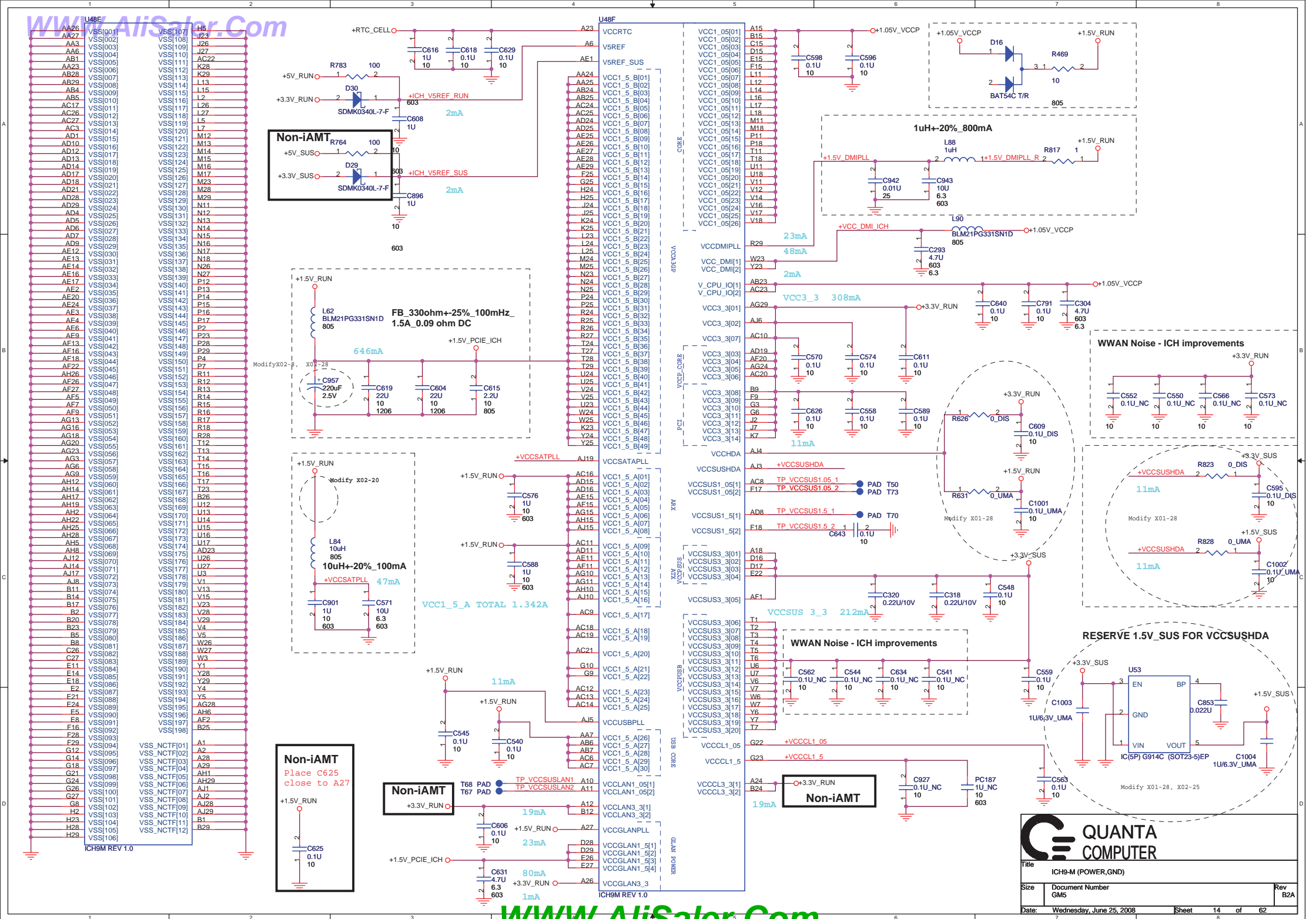




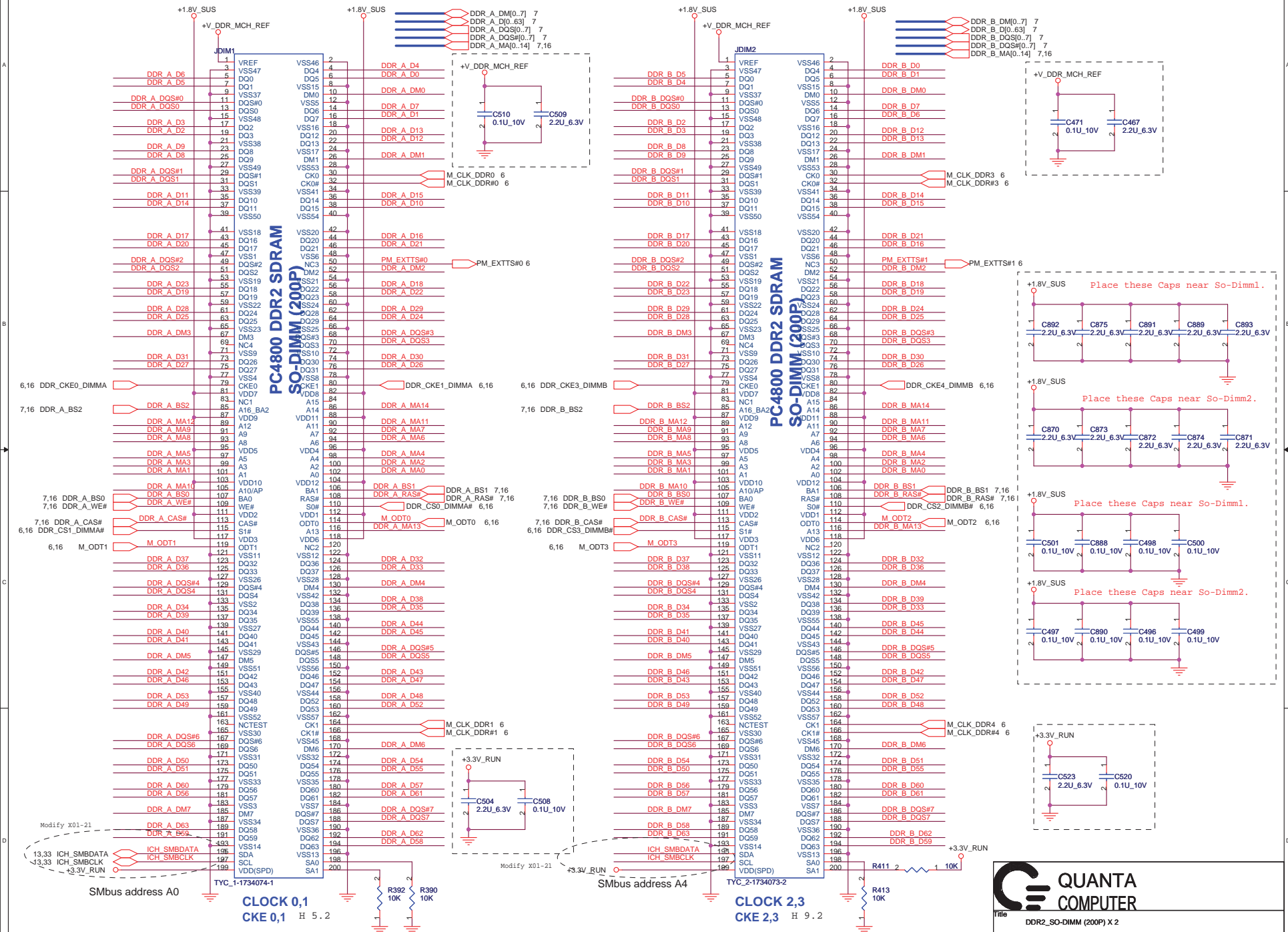
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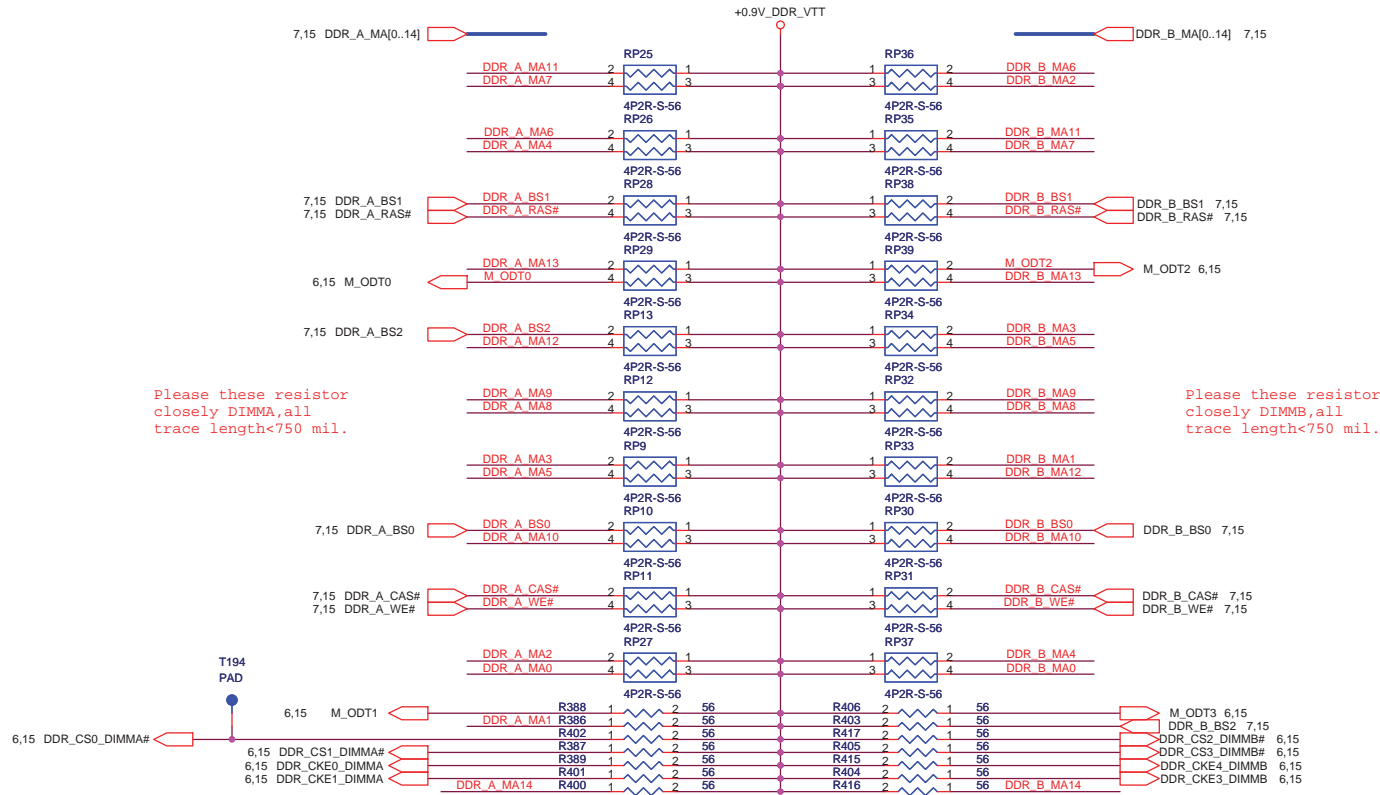
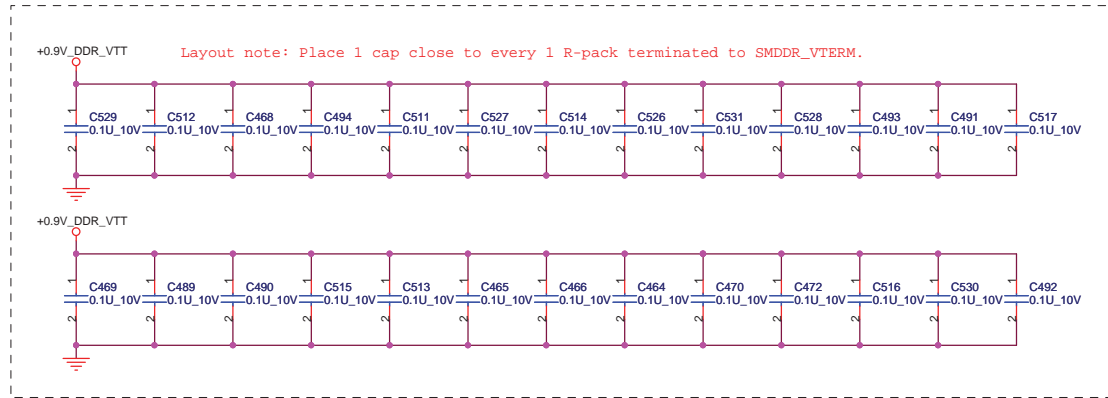




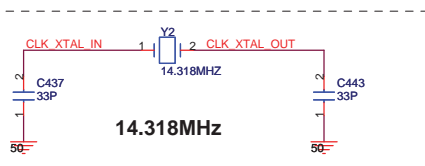


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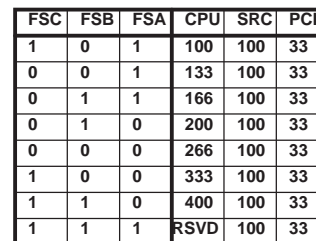




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These are for  
backdrive issue.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL				
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



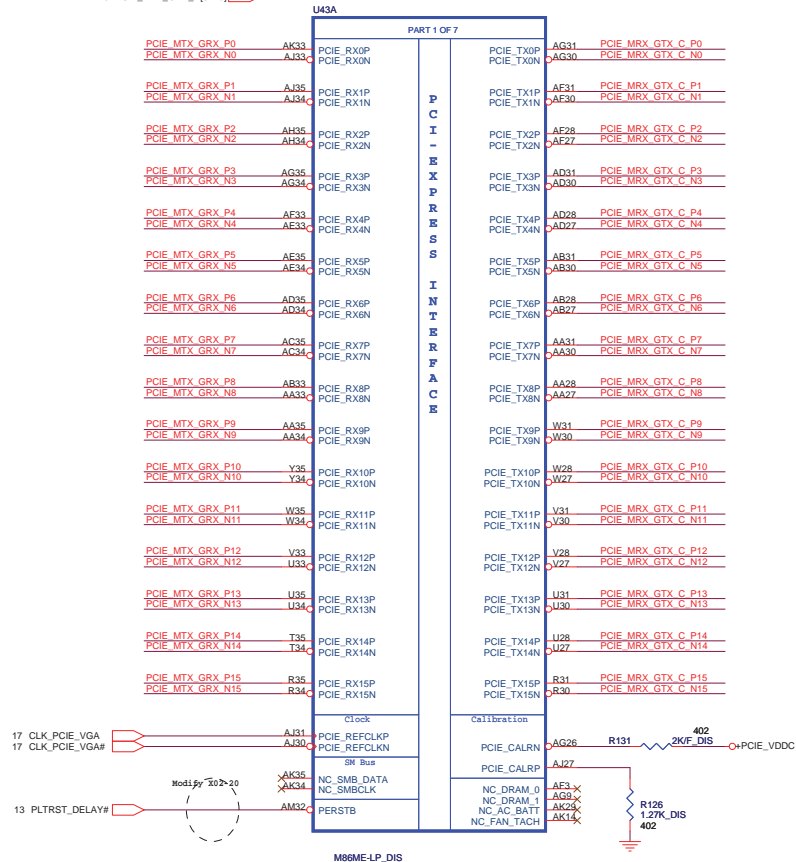
Title  
CLOCK GENERATOR

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6 PCIE\_MTX\_GRP\_P0-15  
6 PCIE\_MTX\_GRP\_N0-15



6 PCIE\_MRX\_GRP\_P0-15  
6 PCIE\_MRX\_GRP\_N0-15

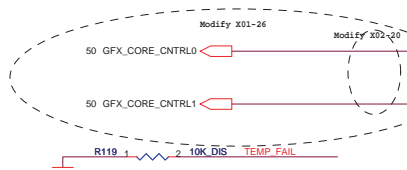
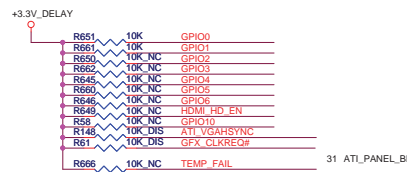
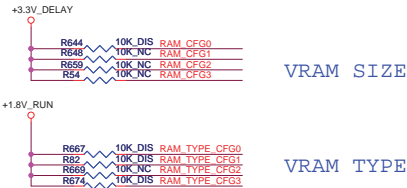




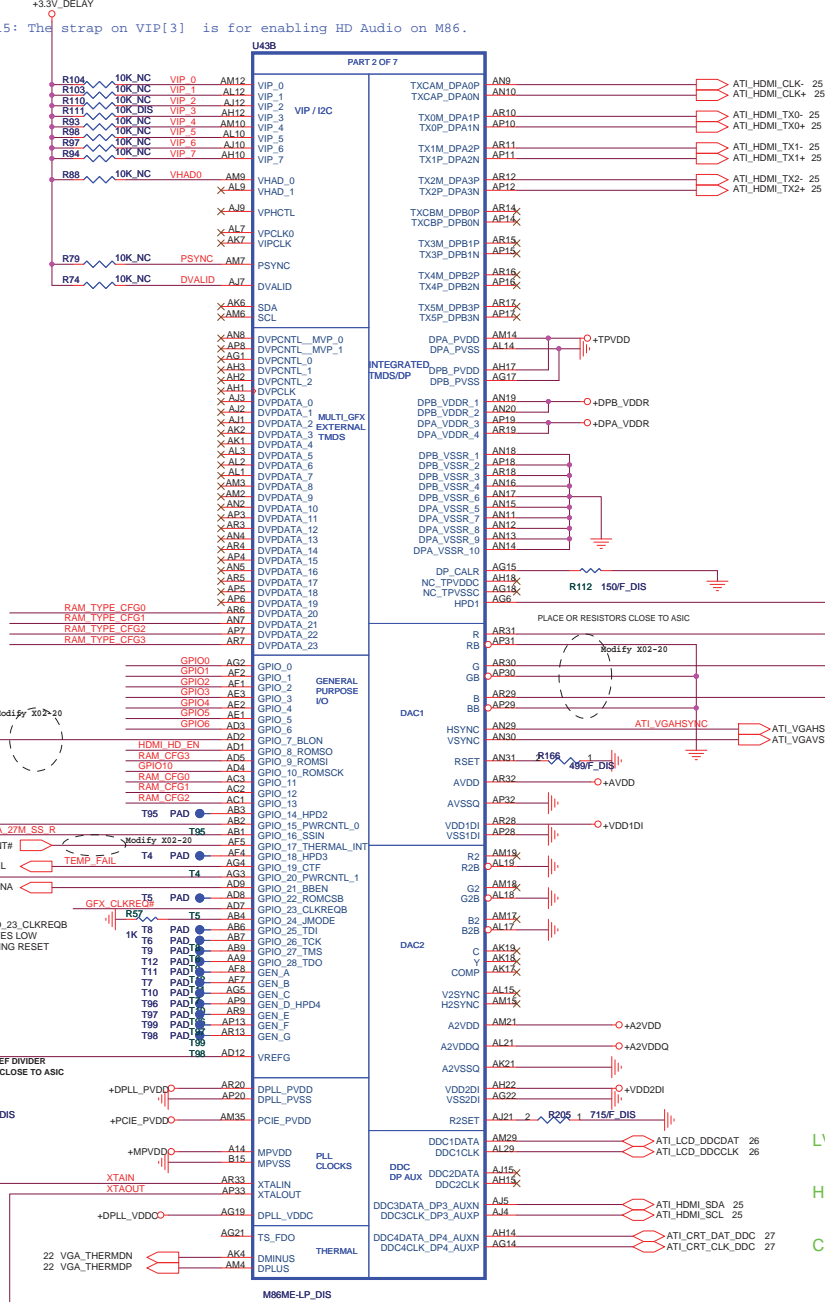
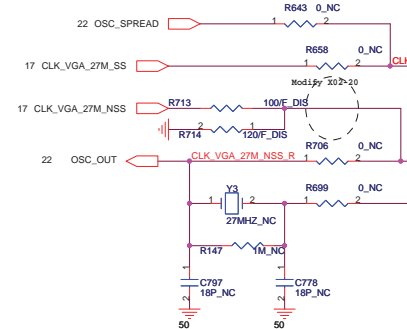
8/15: The strap on VIP[3] is for enabling HD Audio on M86.

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
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256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

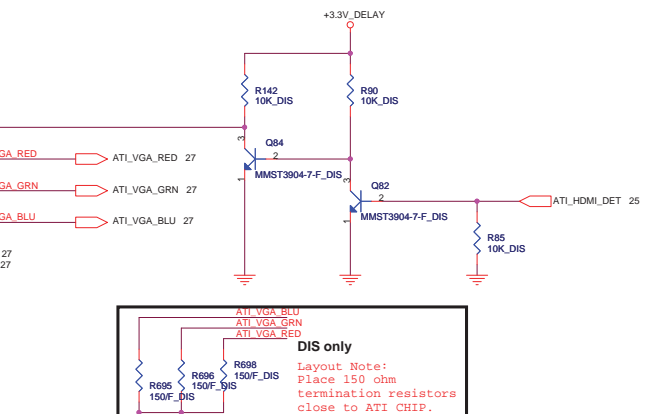
Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
400 MHz 256MB(16M*16) Hynix	1	1	1	1
400 MHz 256MB(16M*16) Qimonda	1	1	1	0
500 MHz 256MB(16M*16) Hynix	1	1	0	1
500 MHz 256MB(16M*16) Qimonda	1	1	0	0
500 MHz 256MB(16M*16) Samsung	1	0	1	1



GFX_CORE_CNTRL_TABLE		
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.1V



HDMI CONN

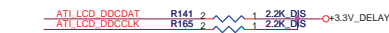


ATI VGA BLU  
ATI VGA GRN  
ATI VGA RED

**DIS only**

Layout Note:  
Place 150 ohm  
termination resistor  
close to ATI CHIP.

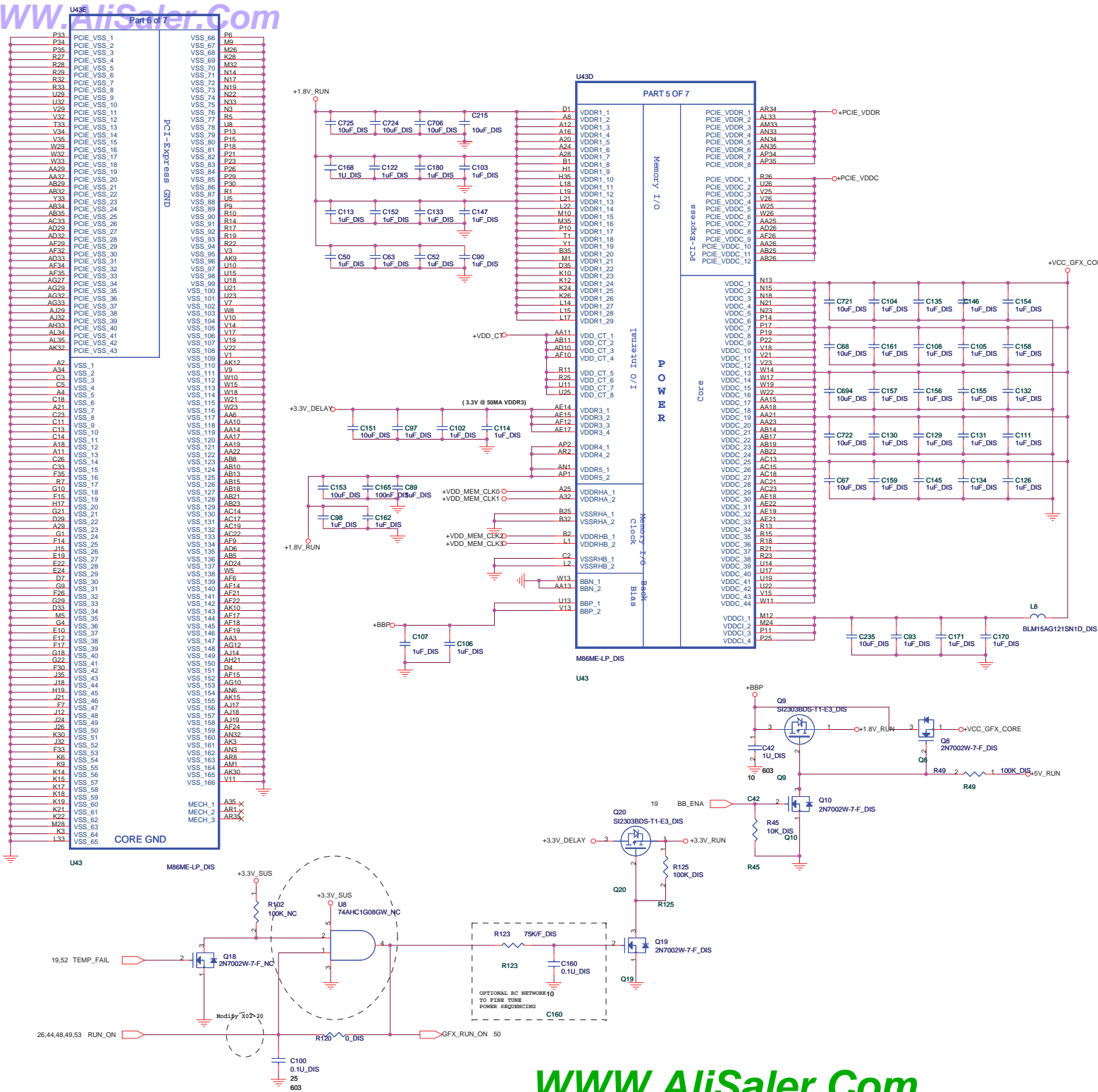
R695 150F\_DIS  
R696 150F\_DIS  
R698 150F\_DIS

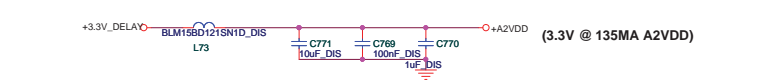
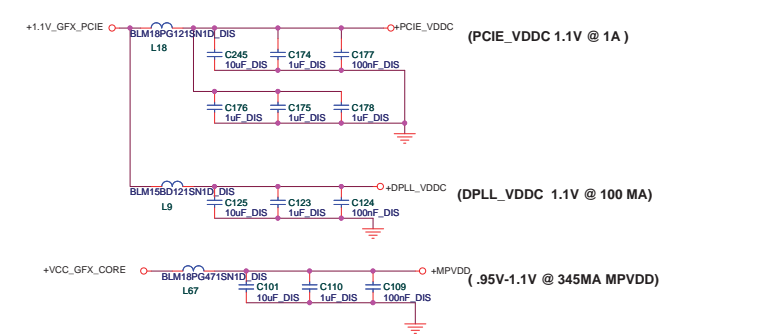
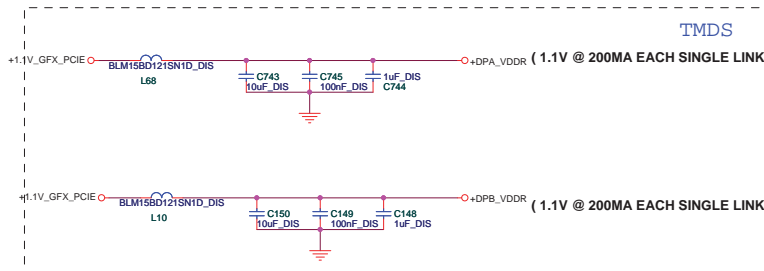
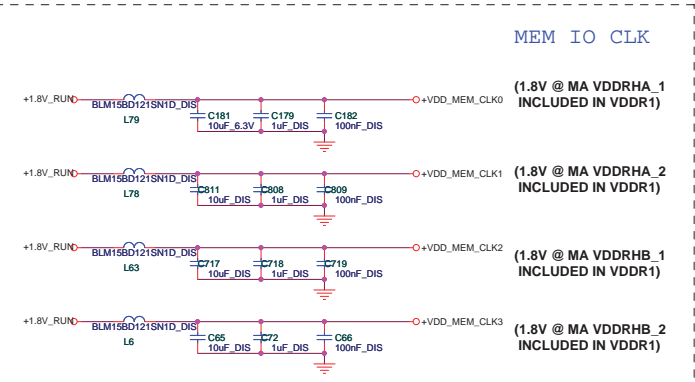
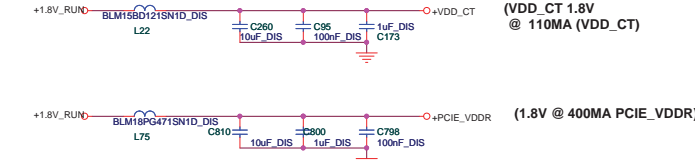
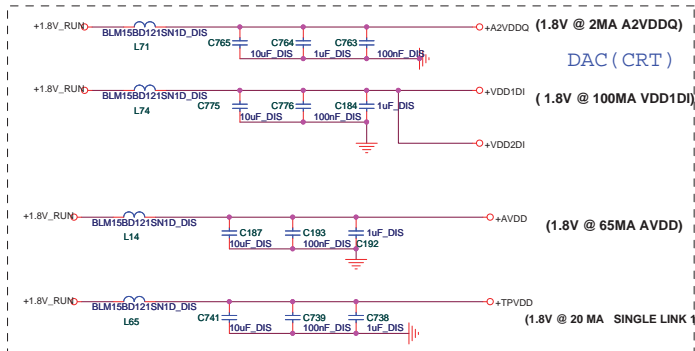
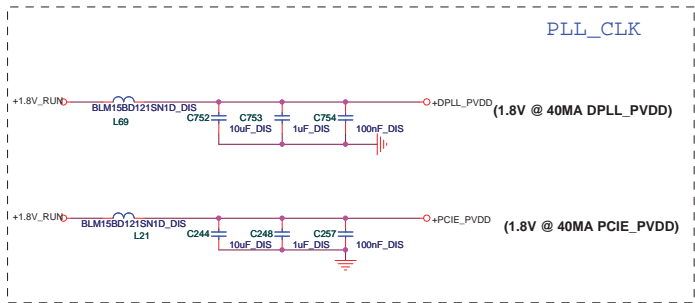
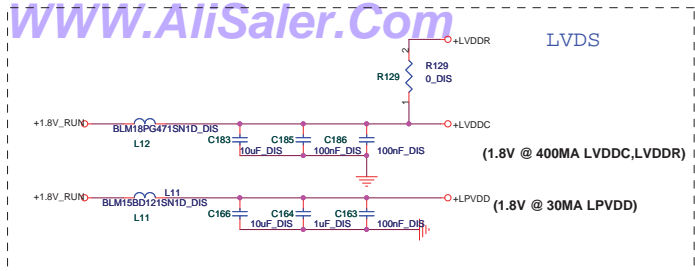


LVDS

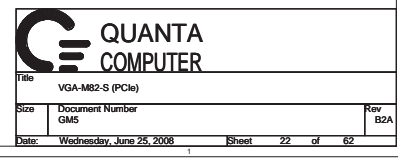
HDMI

CRT

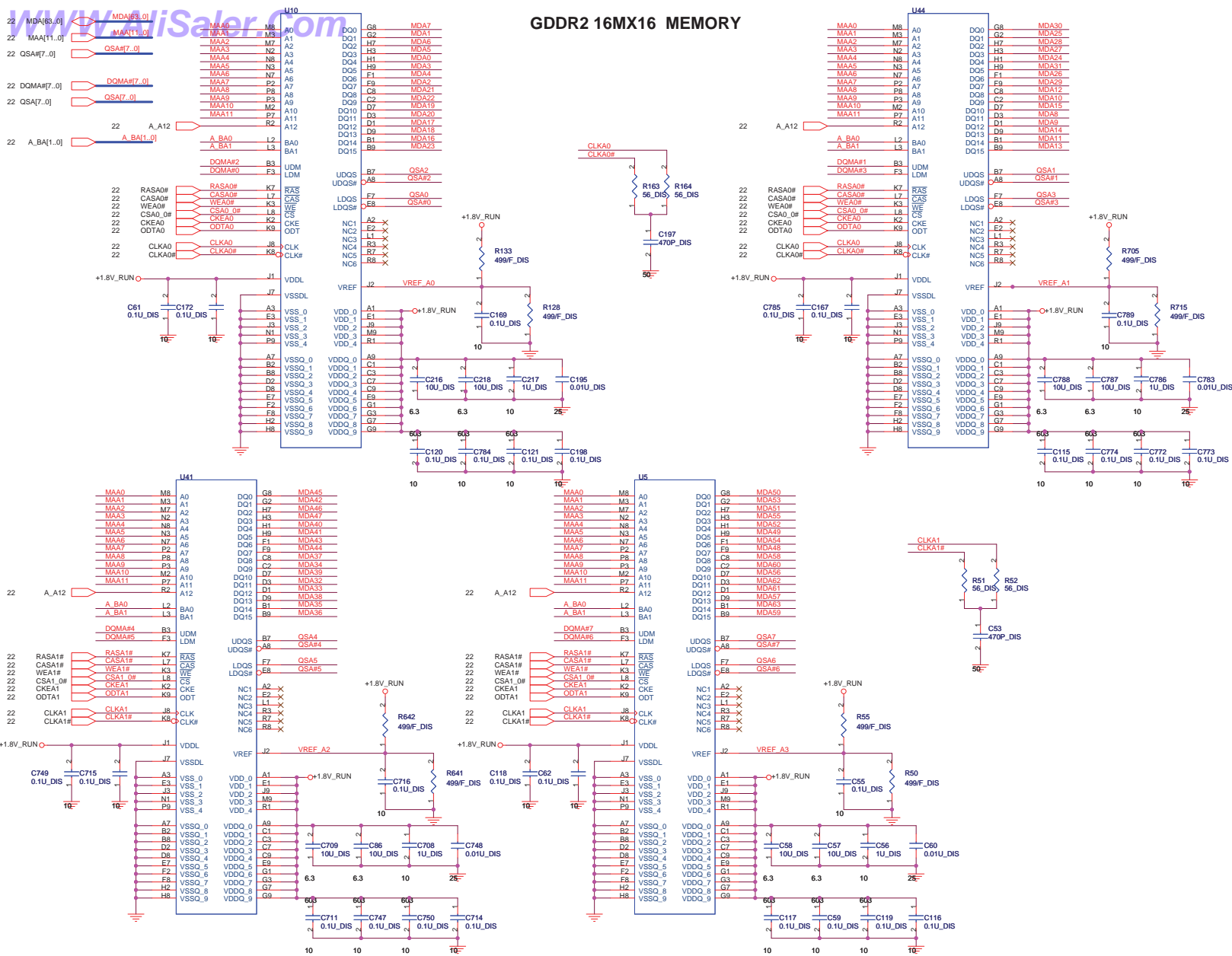




PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

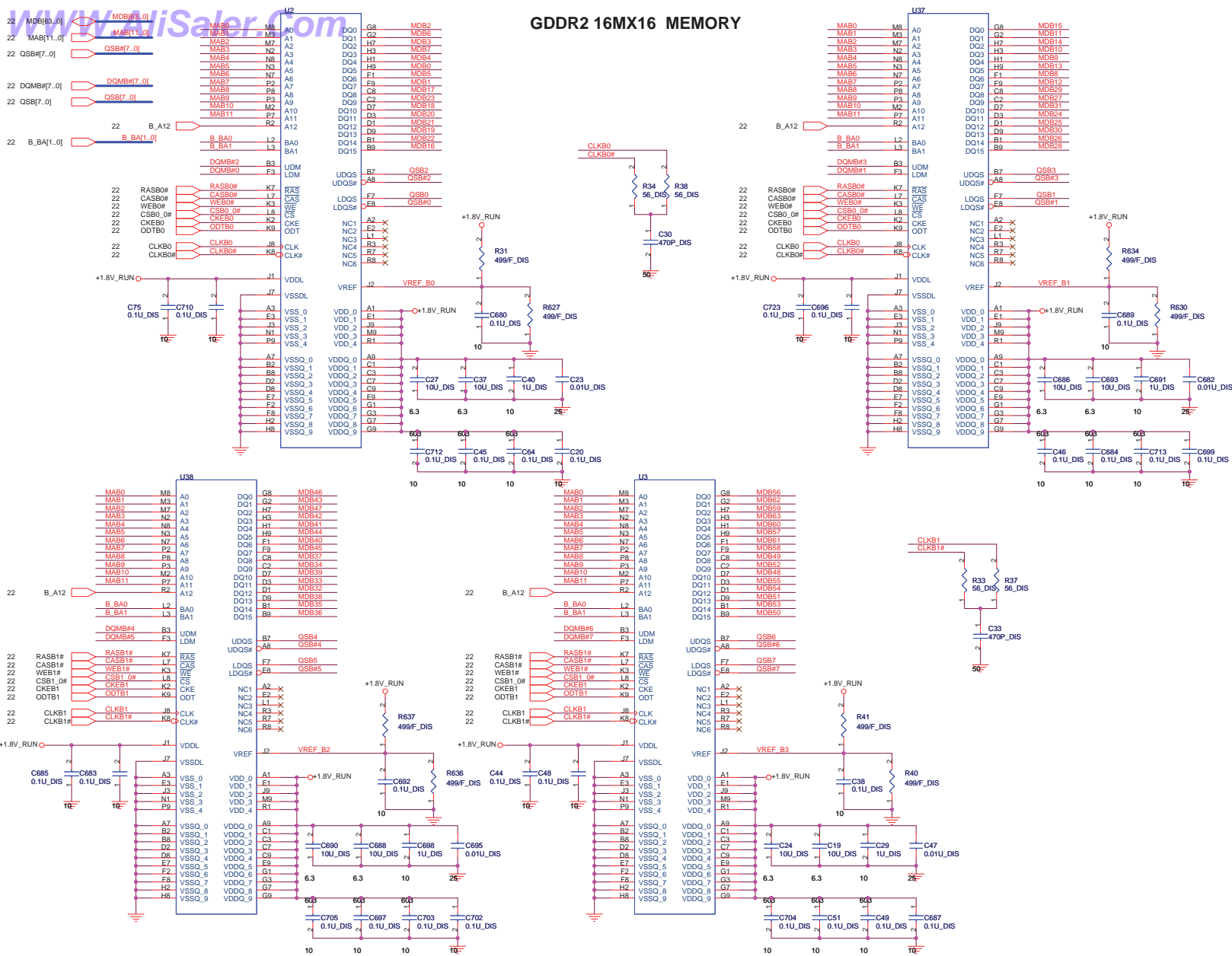


GDDR2 16MX16 MEMORY





GDDR2 16MX16 MEMORY





Title	HDMI PI3VDP411LSZDE
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Size	Document Number
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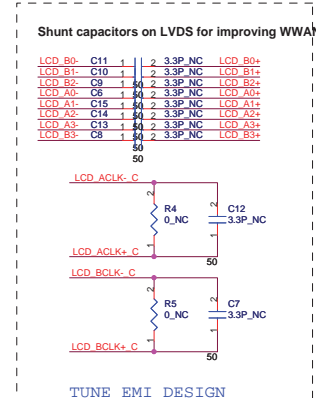
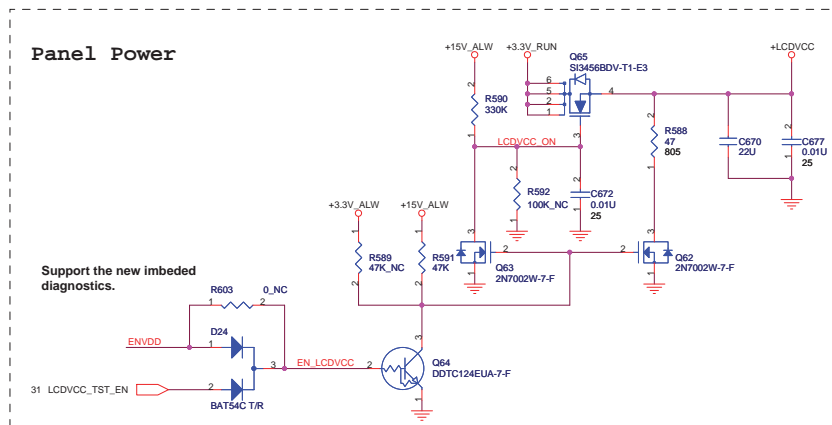
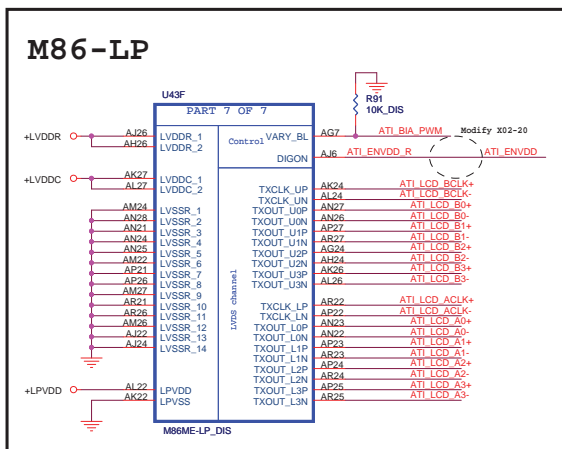
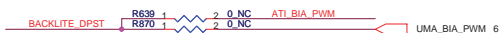
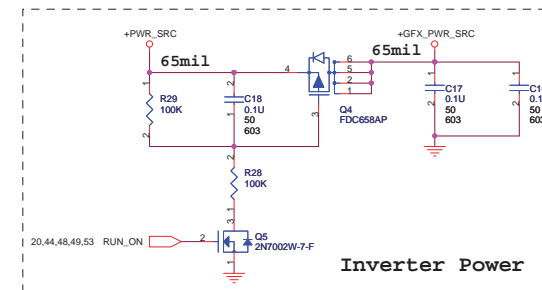
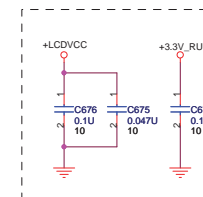
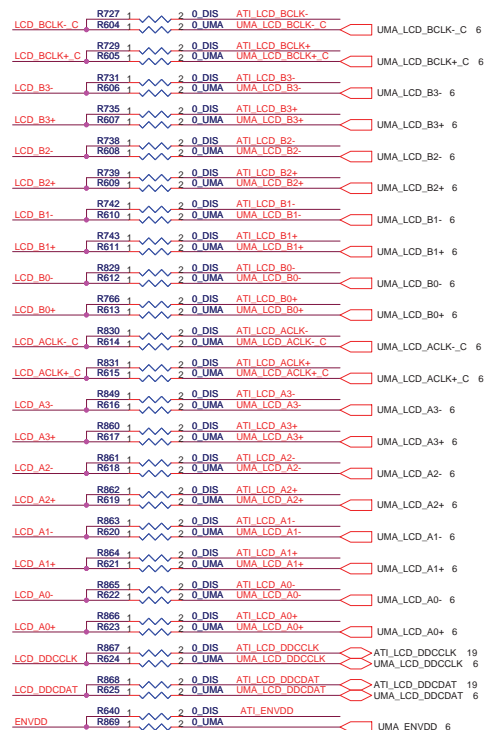
	GM5
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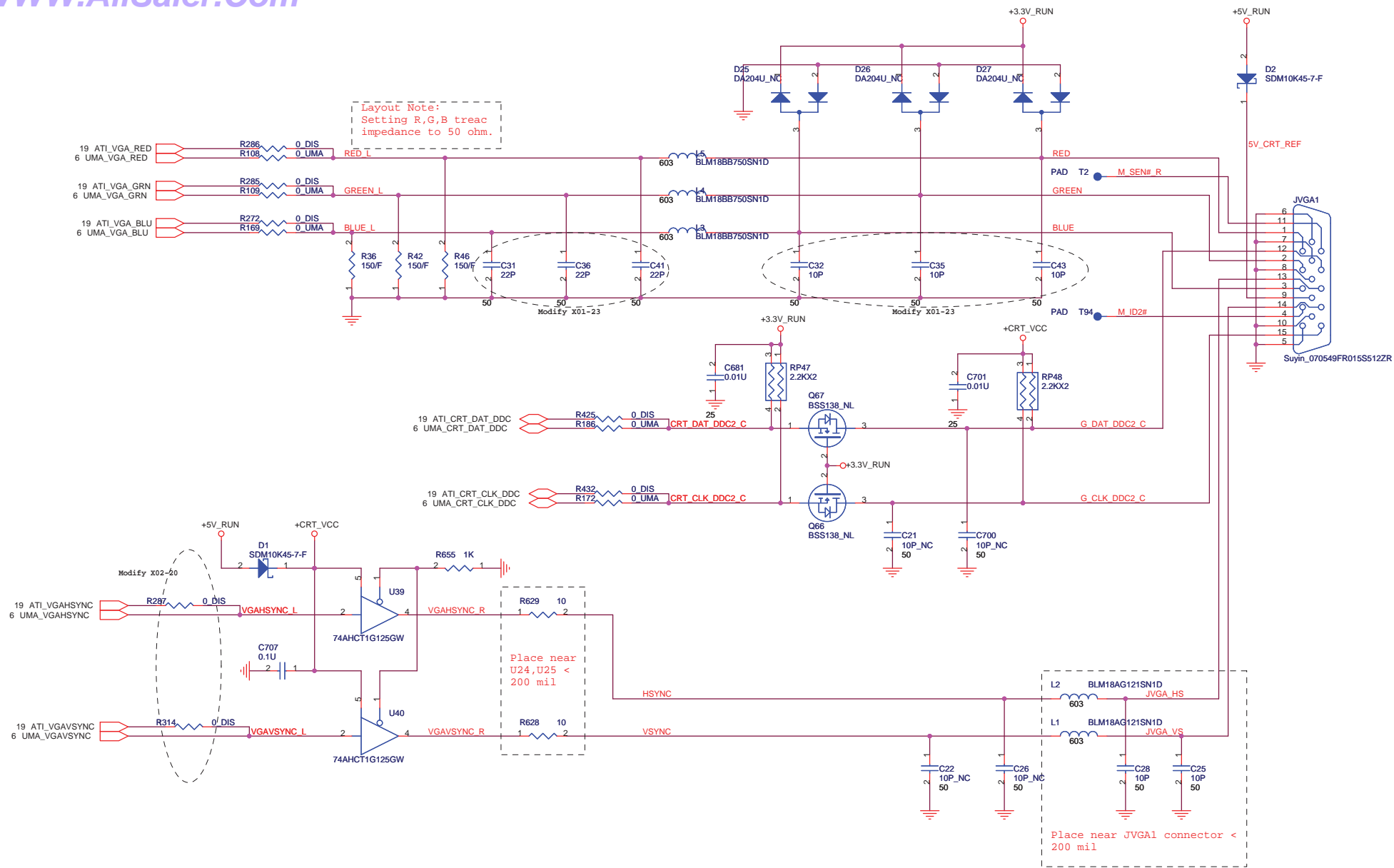
Date: Thursday, June 26.

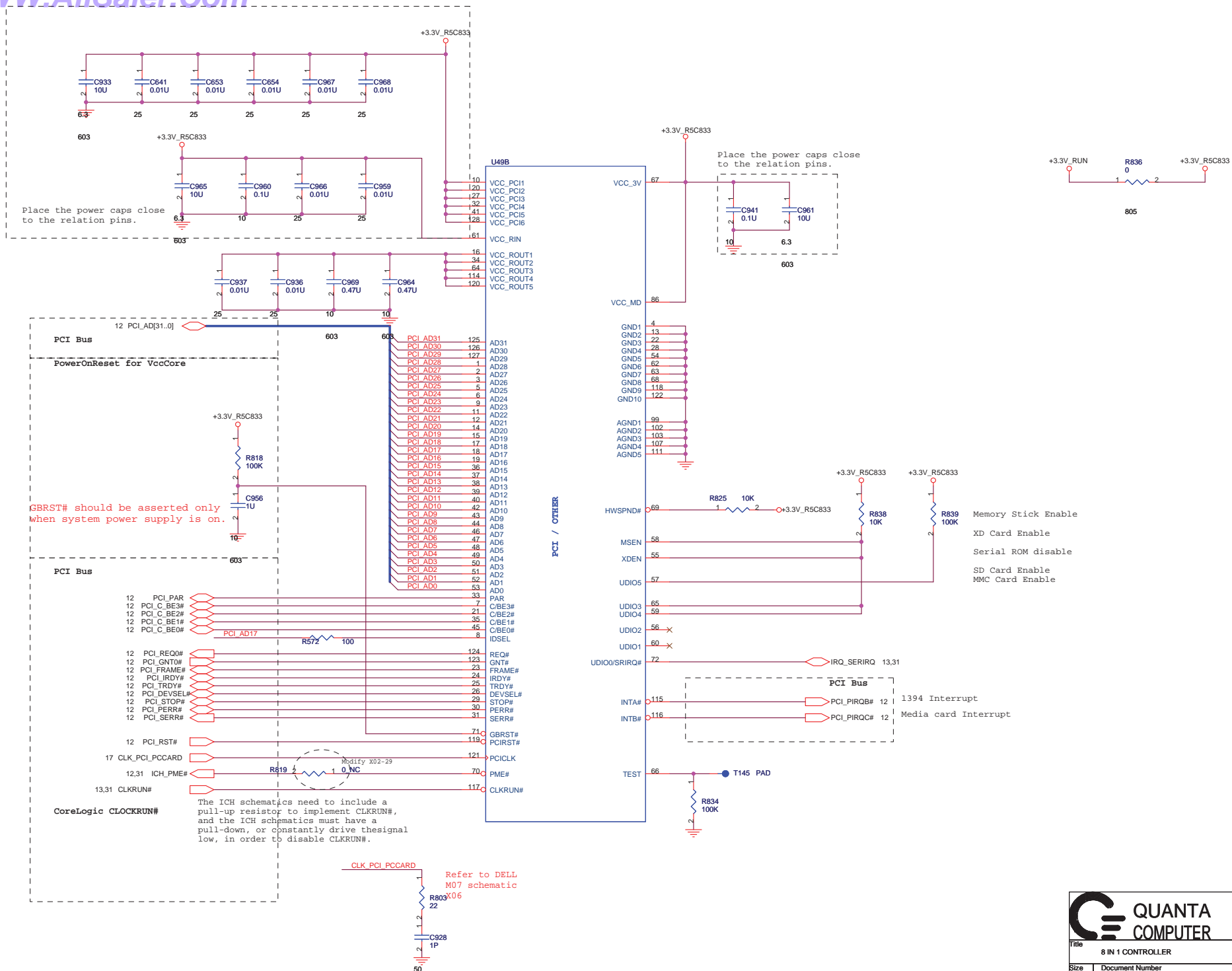
Sheet 25 of 62

Rev

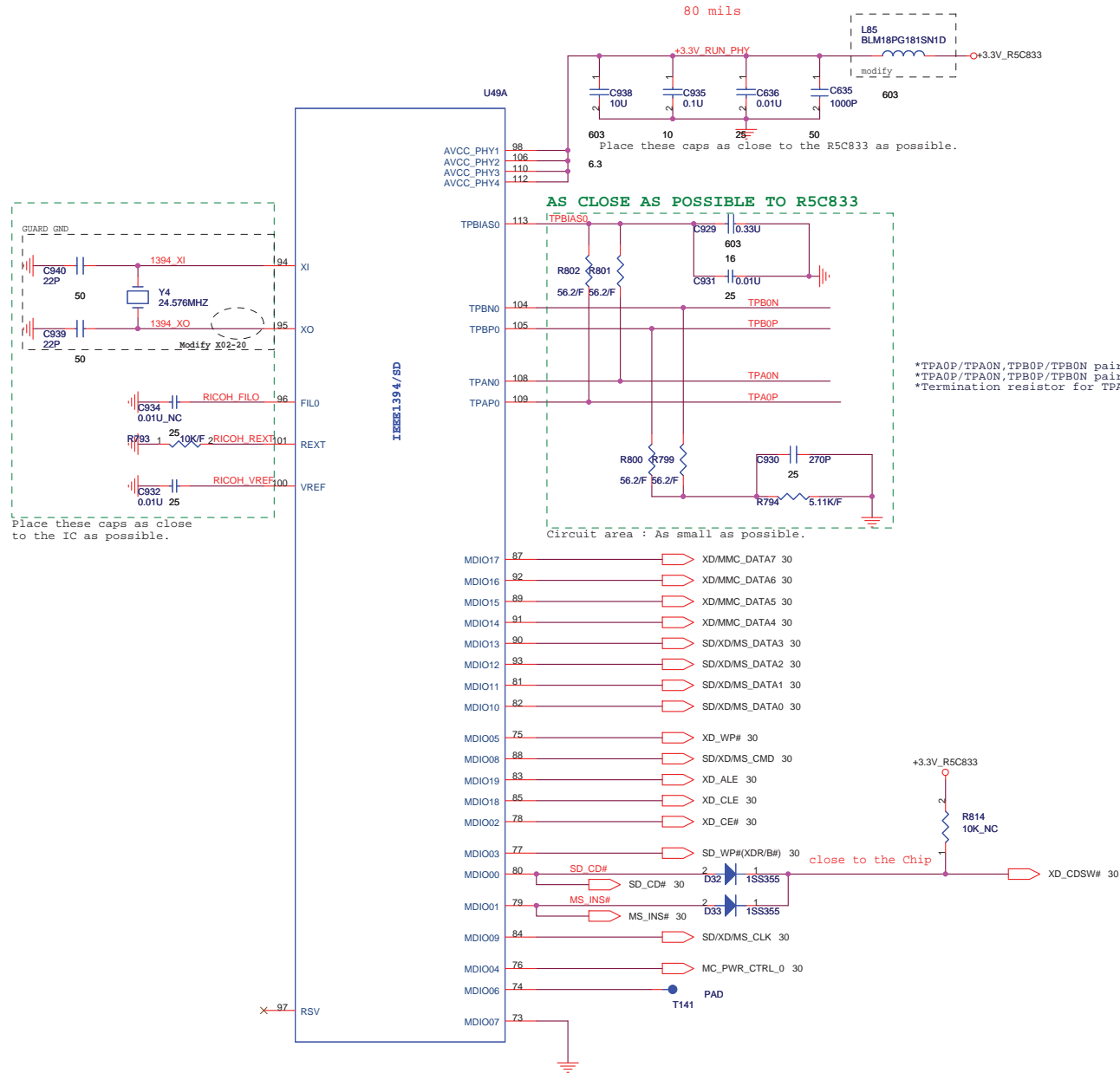
B2A





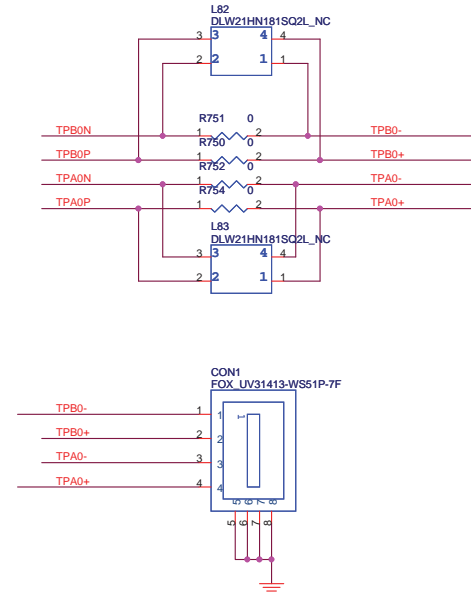




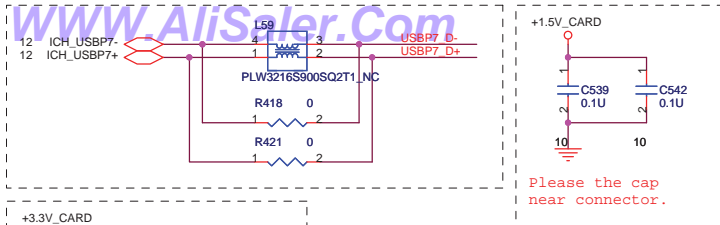


\*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.  
 \*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.  
 \*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

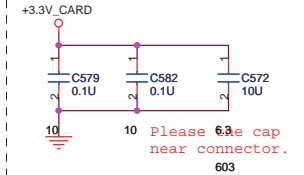
AS CLOSE AS POSSIBLE TO  
1394 CONNECTOR.



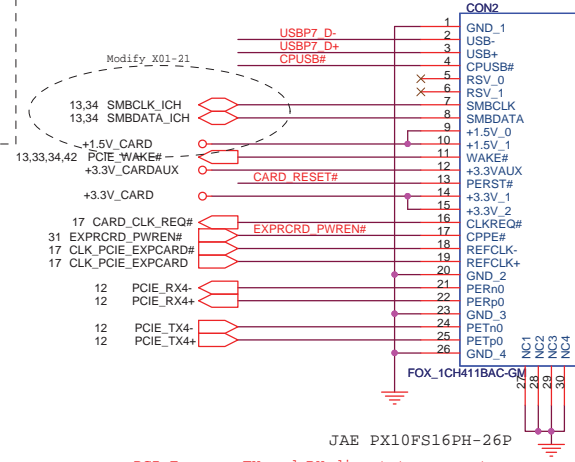
+1.5V\_CARD Max. 650mA, Average 500mA.  
+3V\_CARD Max. 1300mA, Average 1000mA.



Please the cap  
near connector.

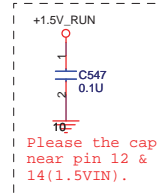
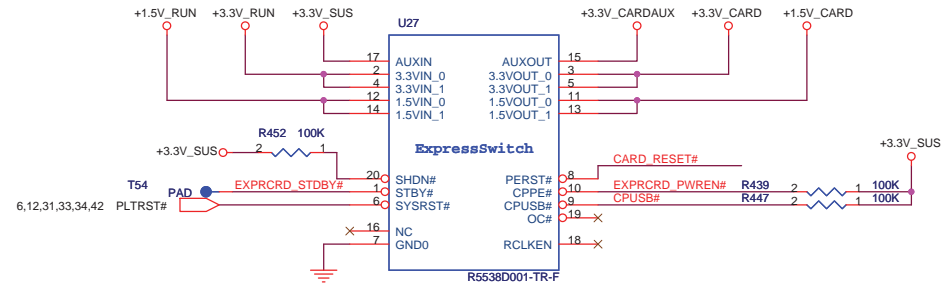


Please ~~6.3~~ cap  
near connector.  
603

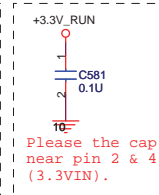


JAE PX10FS16PH-26F

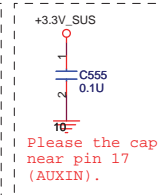
PCI-Express TX and RX direct to connector.



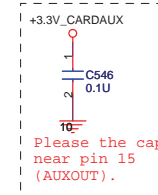
Please the cap  
near pin 12 &  
14(1.5VIN).



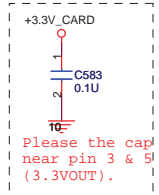
Please the cap  
near pin 2 & 4  
(3.3VIN).



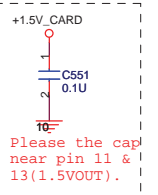
```
| Please the cap  
| near pin 17  
| (AUXIN).
```



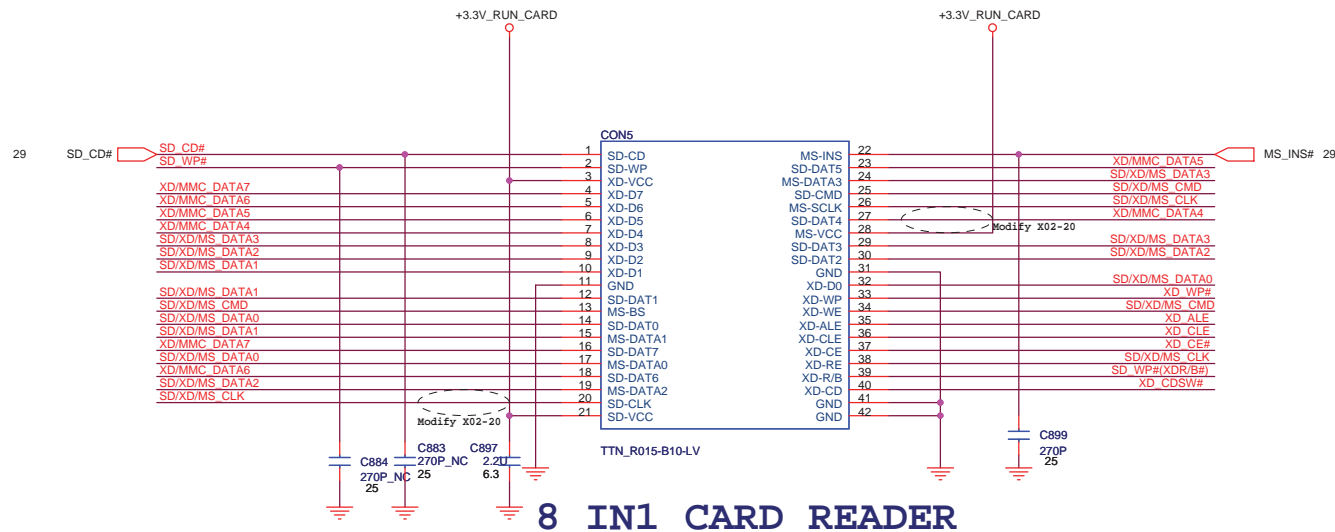
Please the cap  
near pin 15  
(AUXOUT).



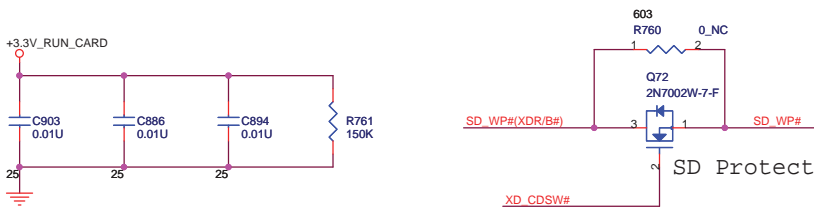
Please the cap  
near pin 3 & 5  
(3.3VOUT).



Please the cap  
near pin 11 &  
13(1.5VOUT).

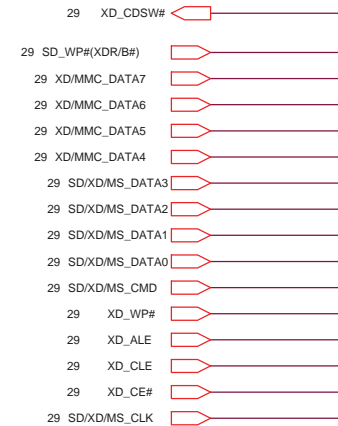
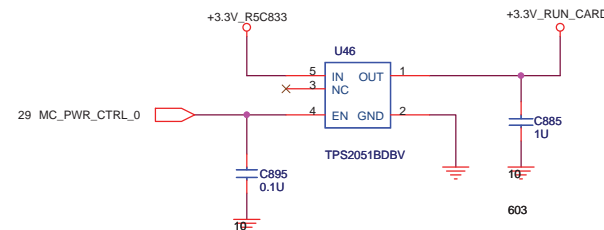


## 8 IN1 CARD READER

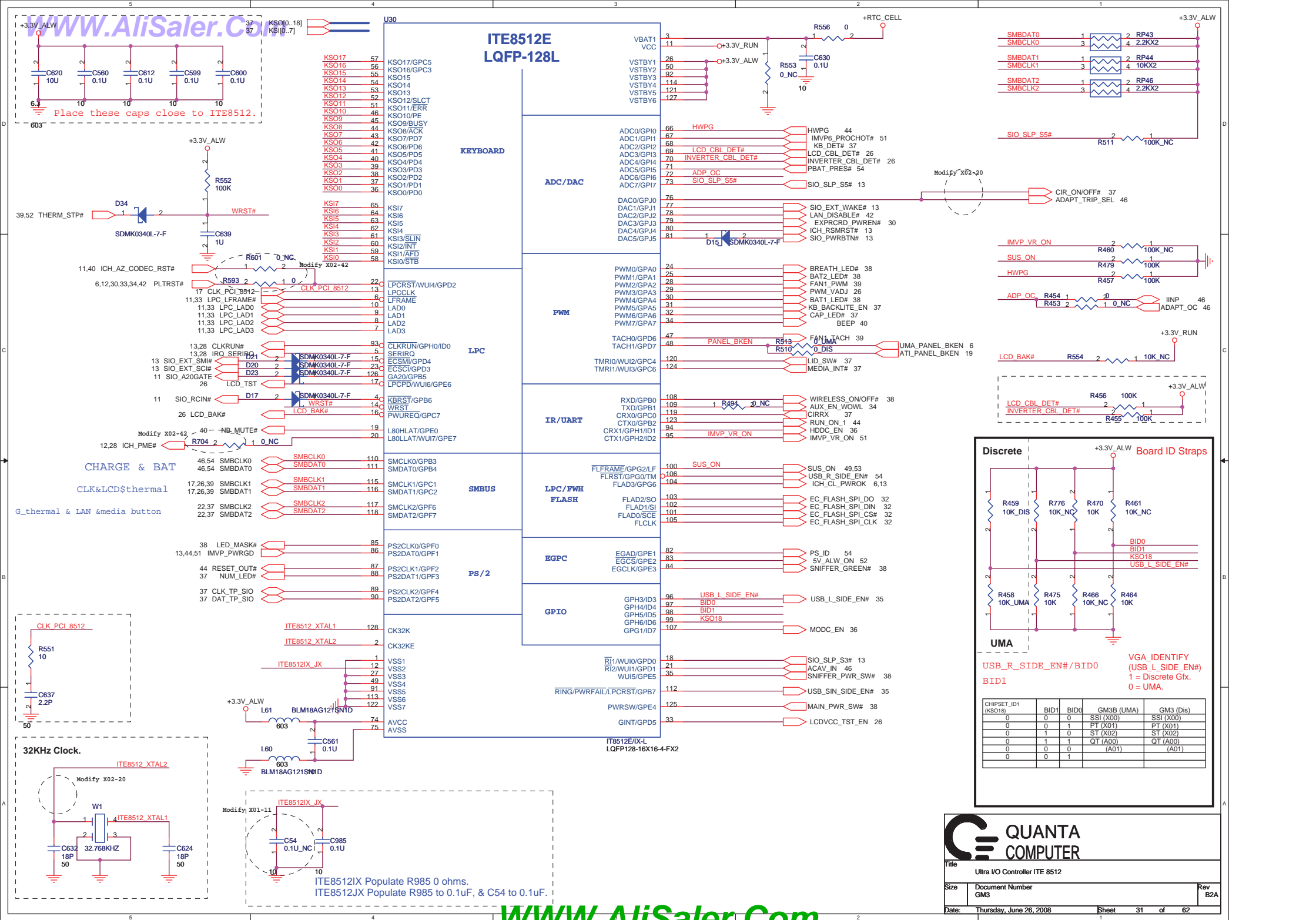


SD Protect

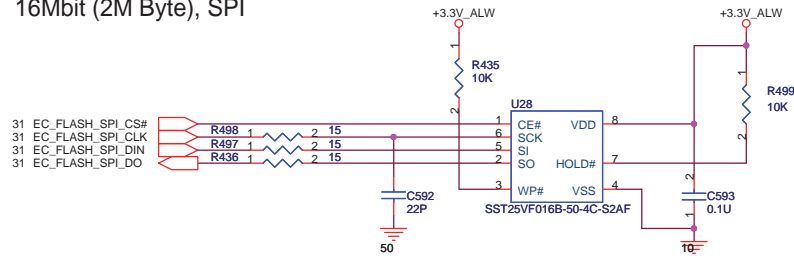
XD\_CDSW#



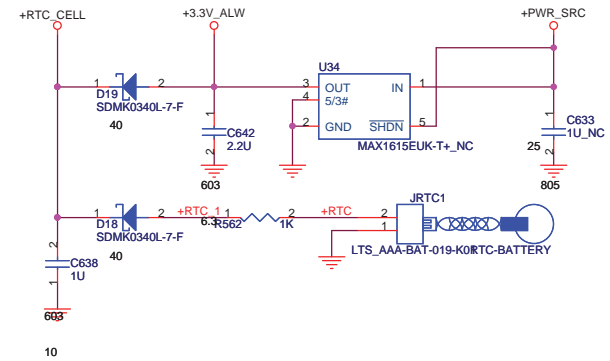
Title			
ExpressCard/SmartCard			
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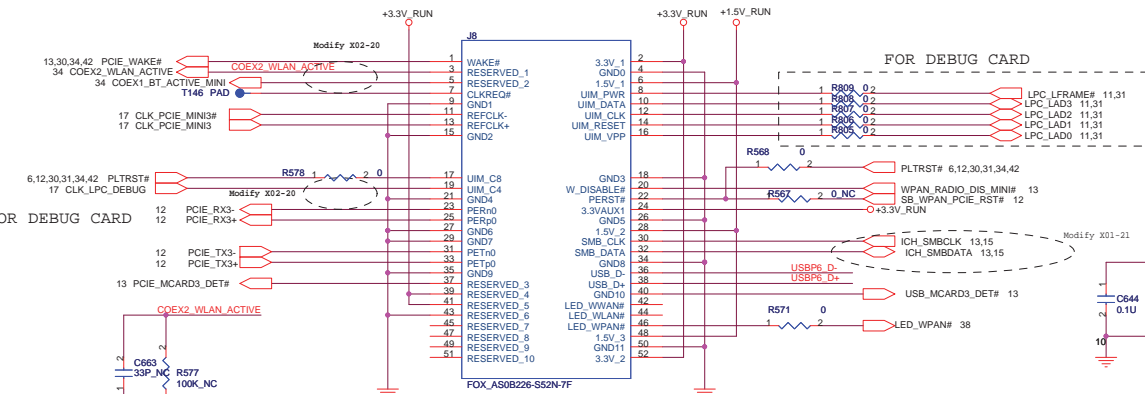
16Mbit (2M Byte), SPI



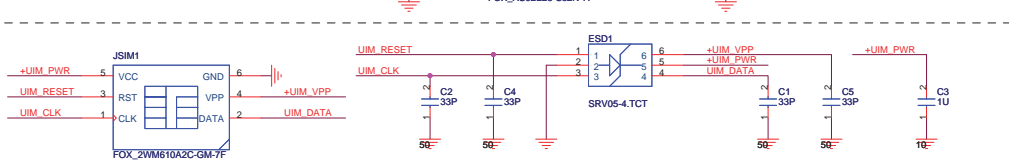
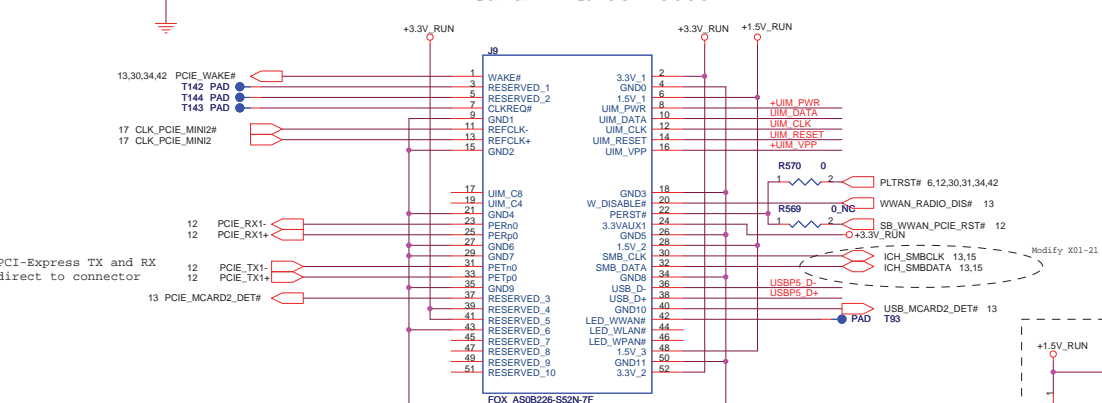
## RTC BATTERY



# MiniCard Robson, UWB connector

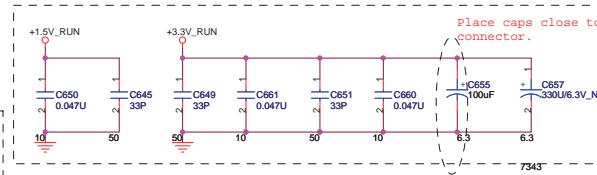
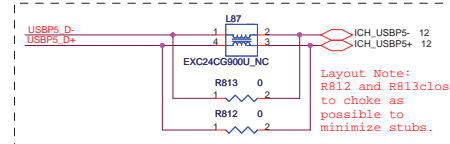
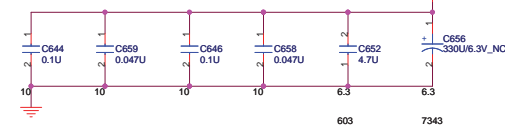
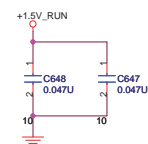
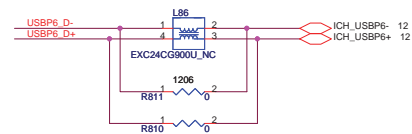


# MiniCard WWAN connector



layout note:10 mil trace and 20 mil space for SIM card and UIM\_PWR use 20mil

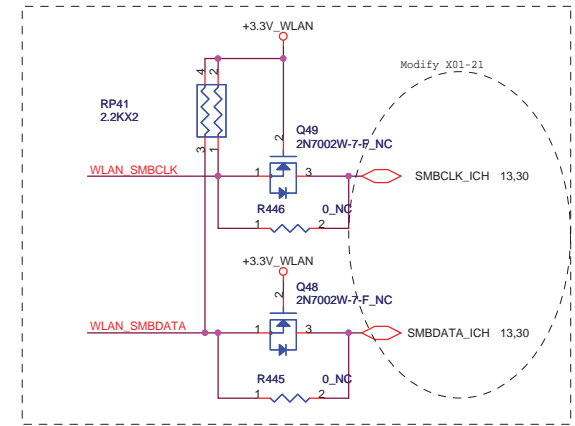
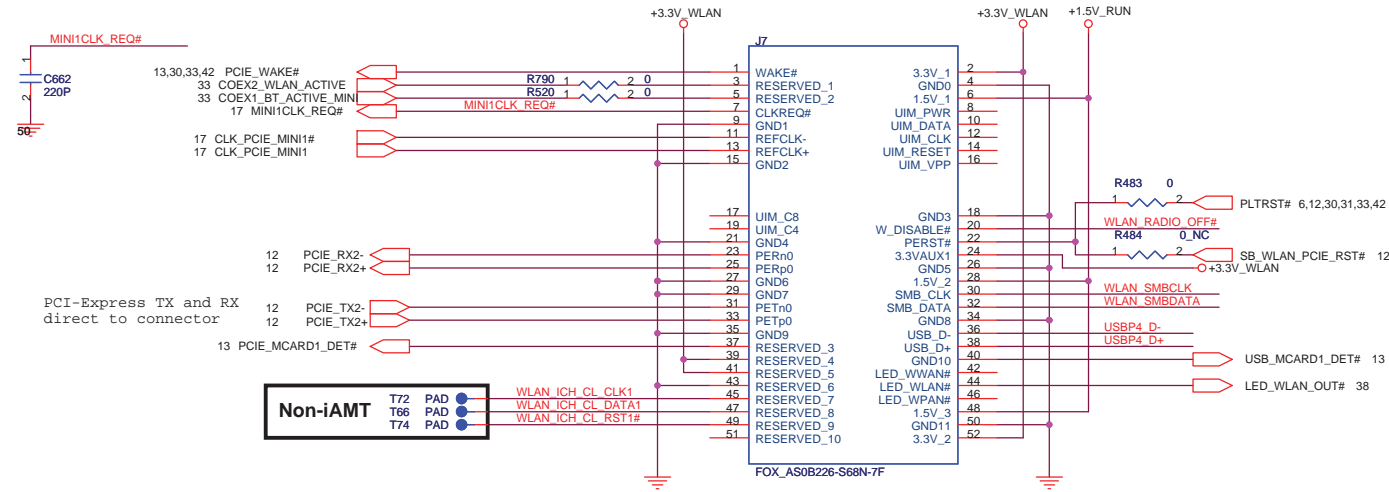
Place as close as possible to WWAN connector



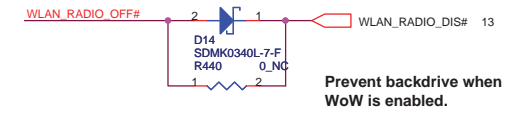
Modify X01-21



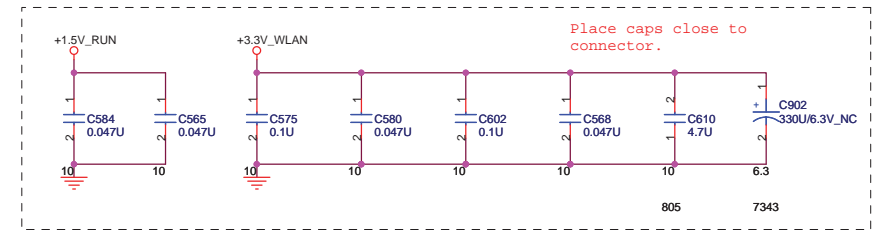
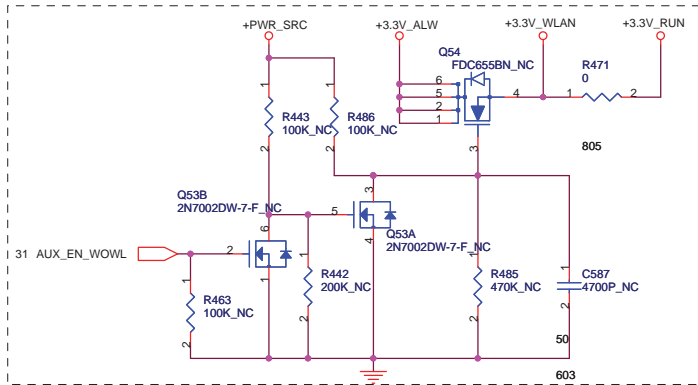
# MiniCard WLAN connector

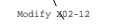
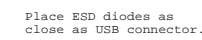
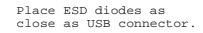
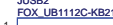


## Support for WoW

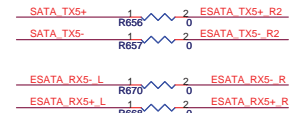


Prevent backdrive when WoW is enabled.



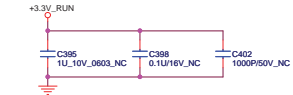
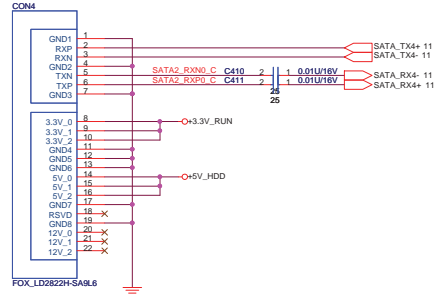


The diagram shows a power plane for a 1.8V supply. A horizontal line represents the power plane, connected to a terminal labeled +1.8V\_RUN. Below this line, four capacitors are connected in parallel to a common ground line. The capacitors are labeled C1006, C1007, C1008, and C1009. Each capacitor has a value of 0.1U and a voltage rating of 10V\_NC.

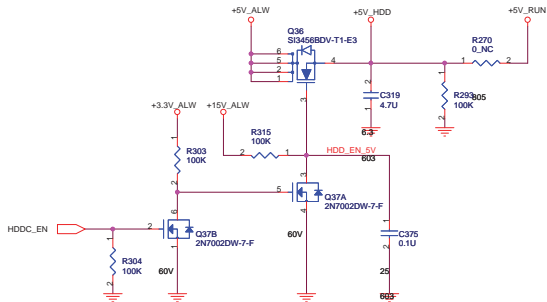


Title			
External USB			
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Date:	Wednesday, June 25, 2008	Sheet	35 of 62

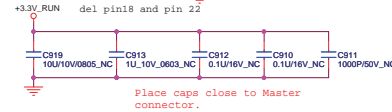
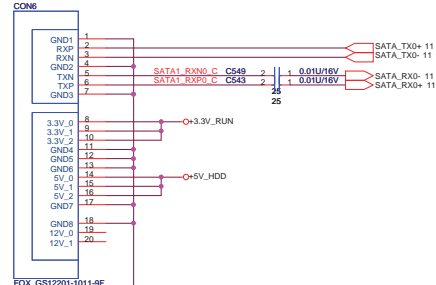
SATA Connector.



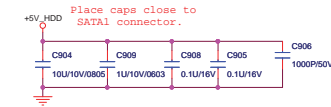
Place caps close to Second HDD connector.



Master

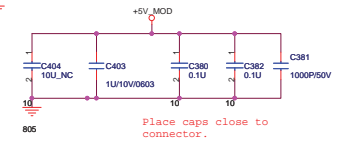
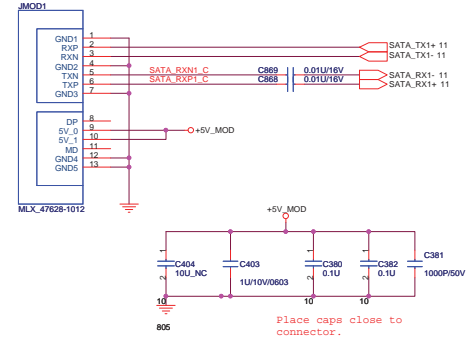


Place caps close to Master connector.

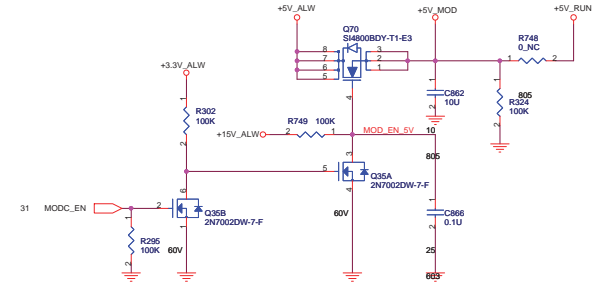


Place caps close to SATA1 connector.

ODD Connector

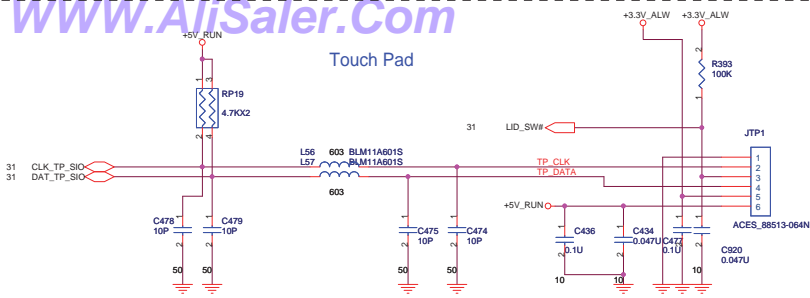


Place caps close to connector.

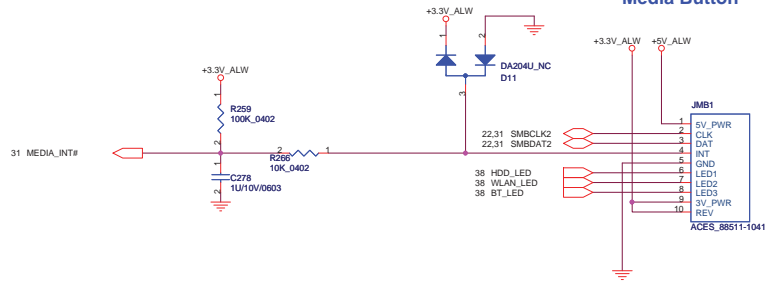


File	SATA (HDD&CD_ROM)	Rev	B2A
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Date	Wednesday, June 25, 2008	Sheet	38 of 62

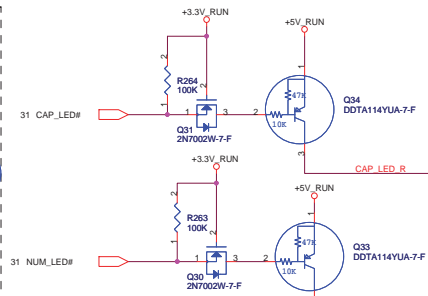
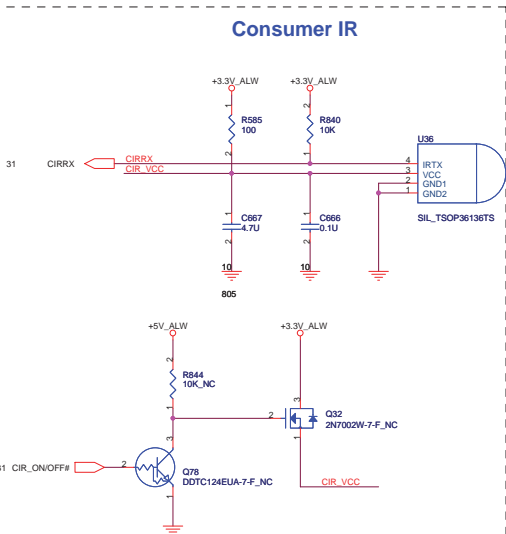
### Touch Pad



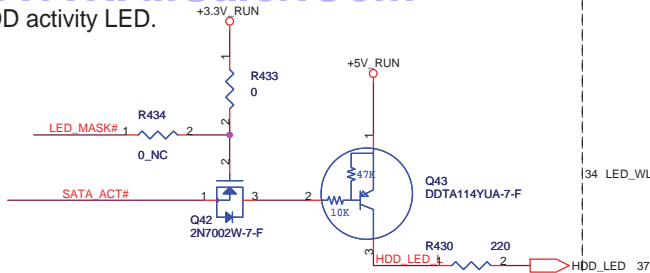
### Media Button



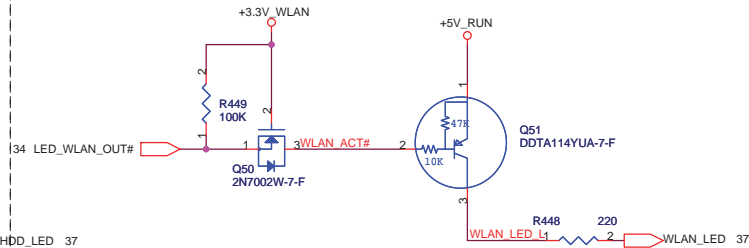
### Consumer IR



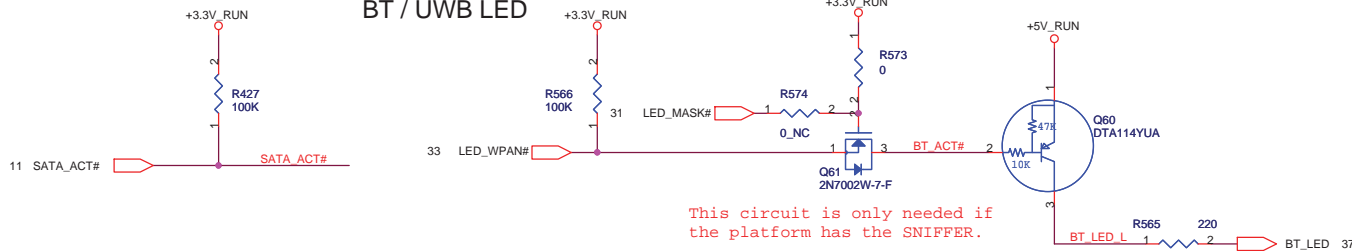
# HDD activity LED.



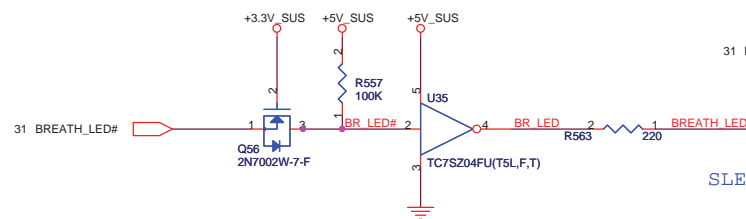
# WLAN



# BT / UWB LED

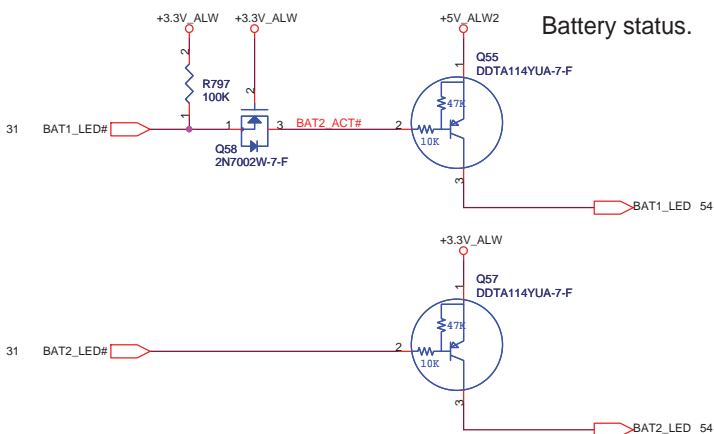


# Power & Suspend.

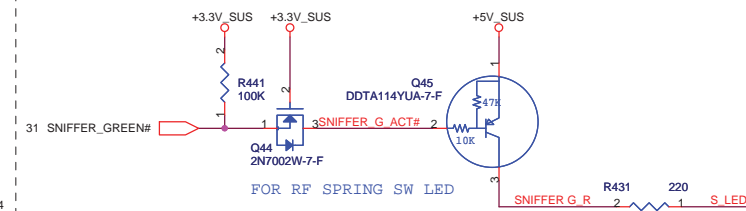


SLED2:AP detection

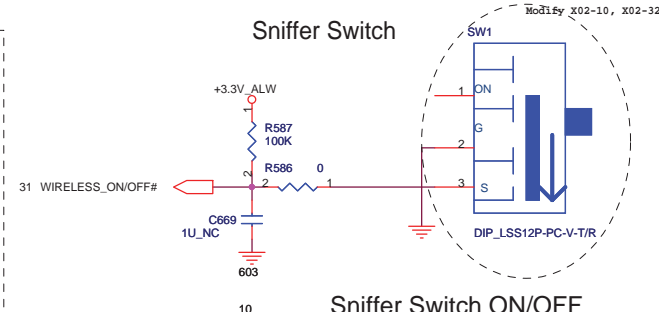
# Battery status.



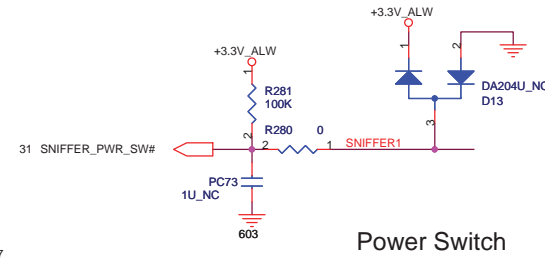
# Sniffer LED



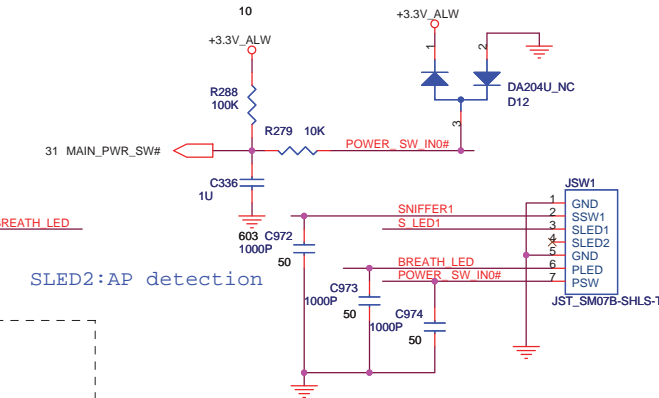
# Sniffer Switch



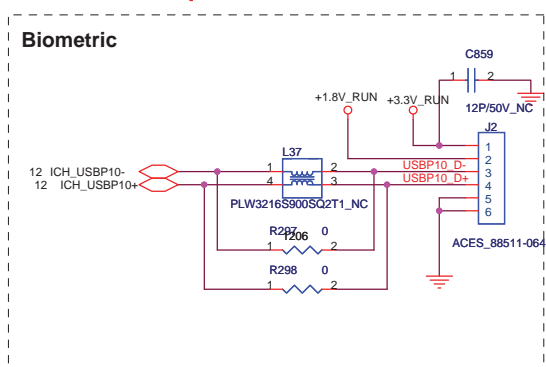
# Sniffer Switch ON/OFF



# Power Switch

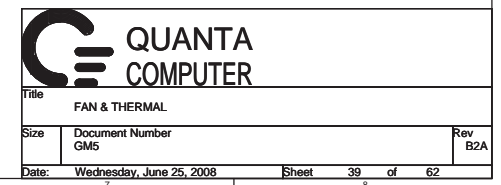


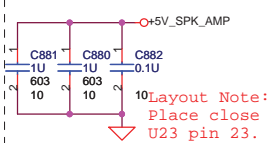
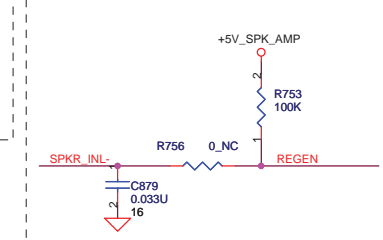
# Biometric



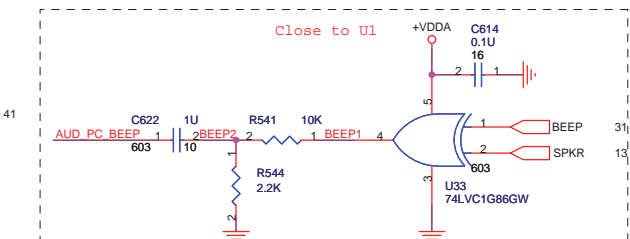
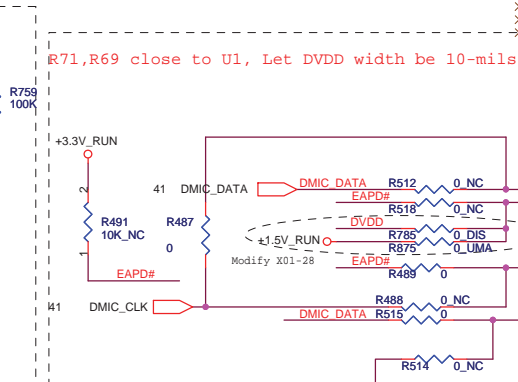
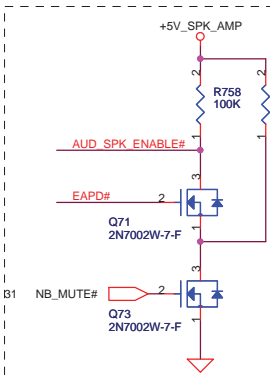
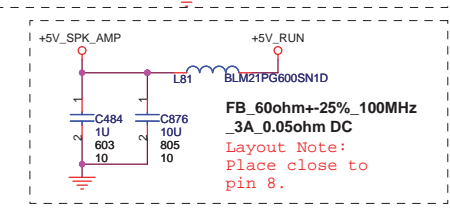
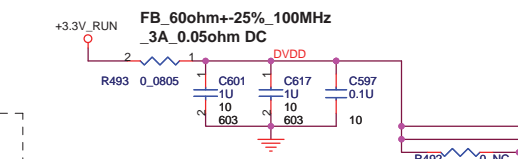
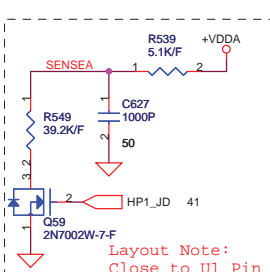
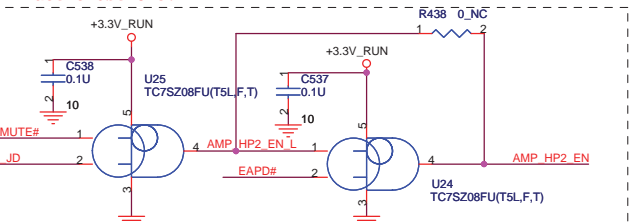
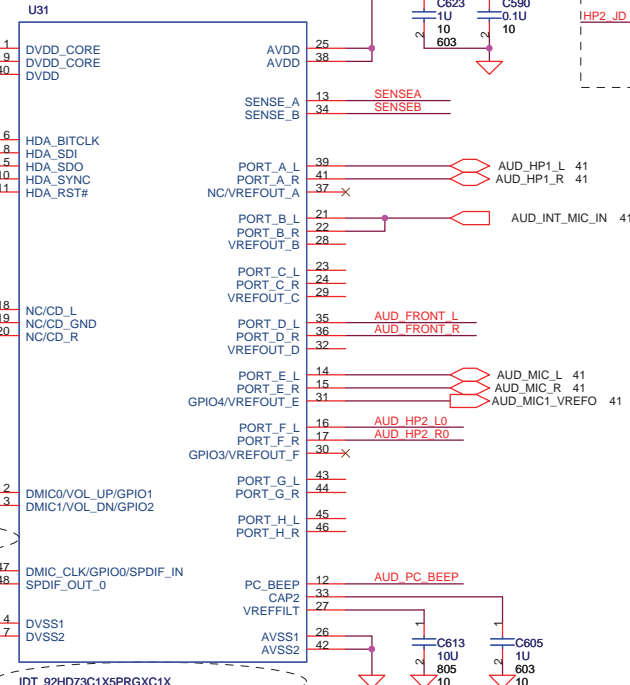
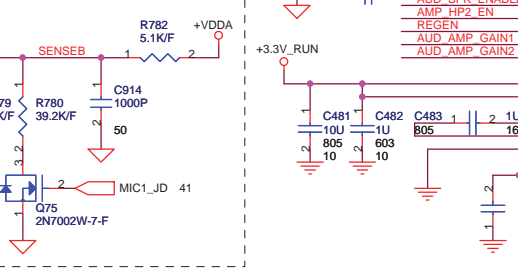
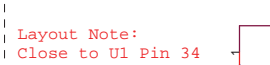
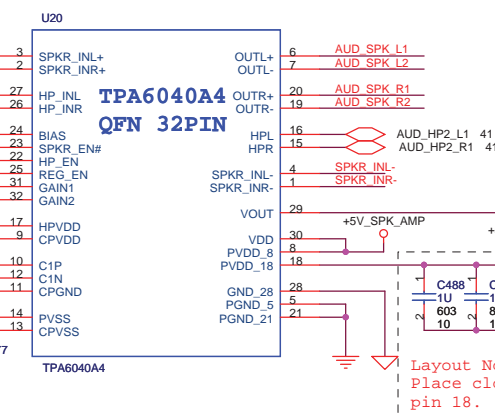
Title			SWITCH, KEYBOARD & LED
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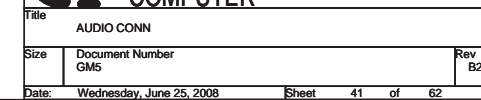
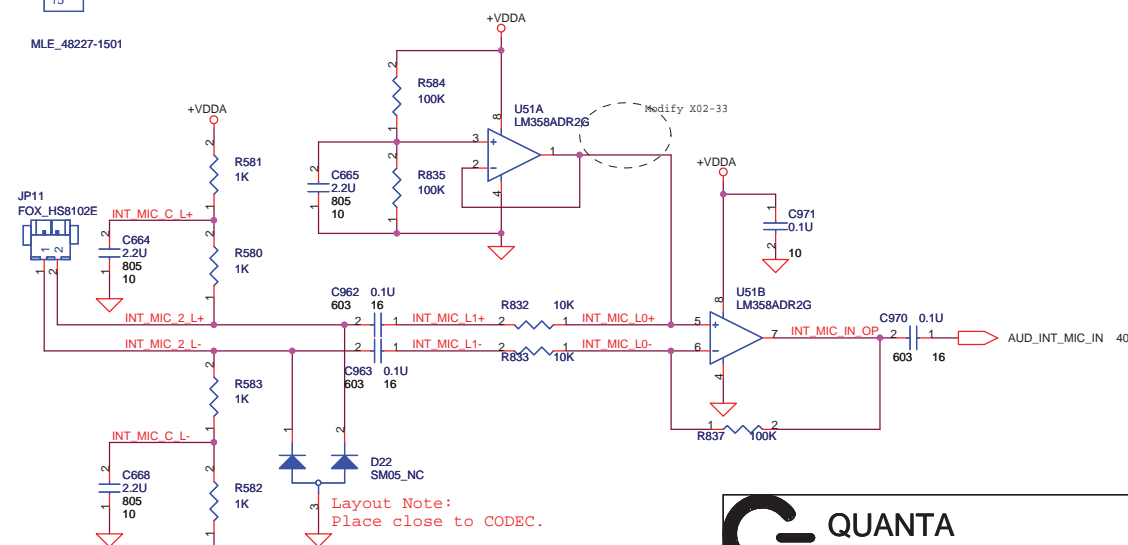
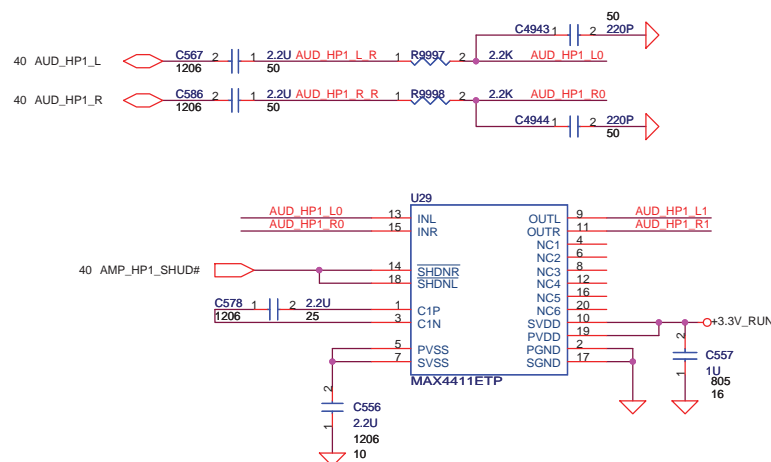


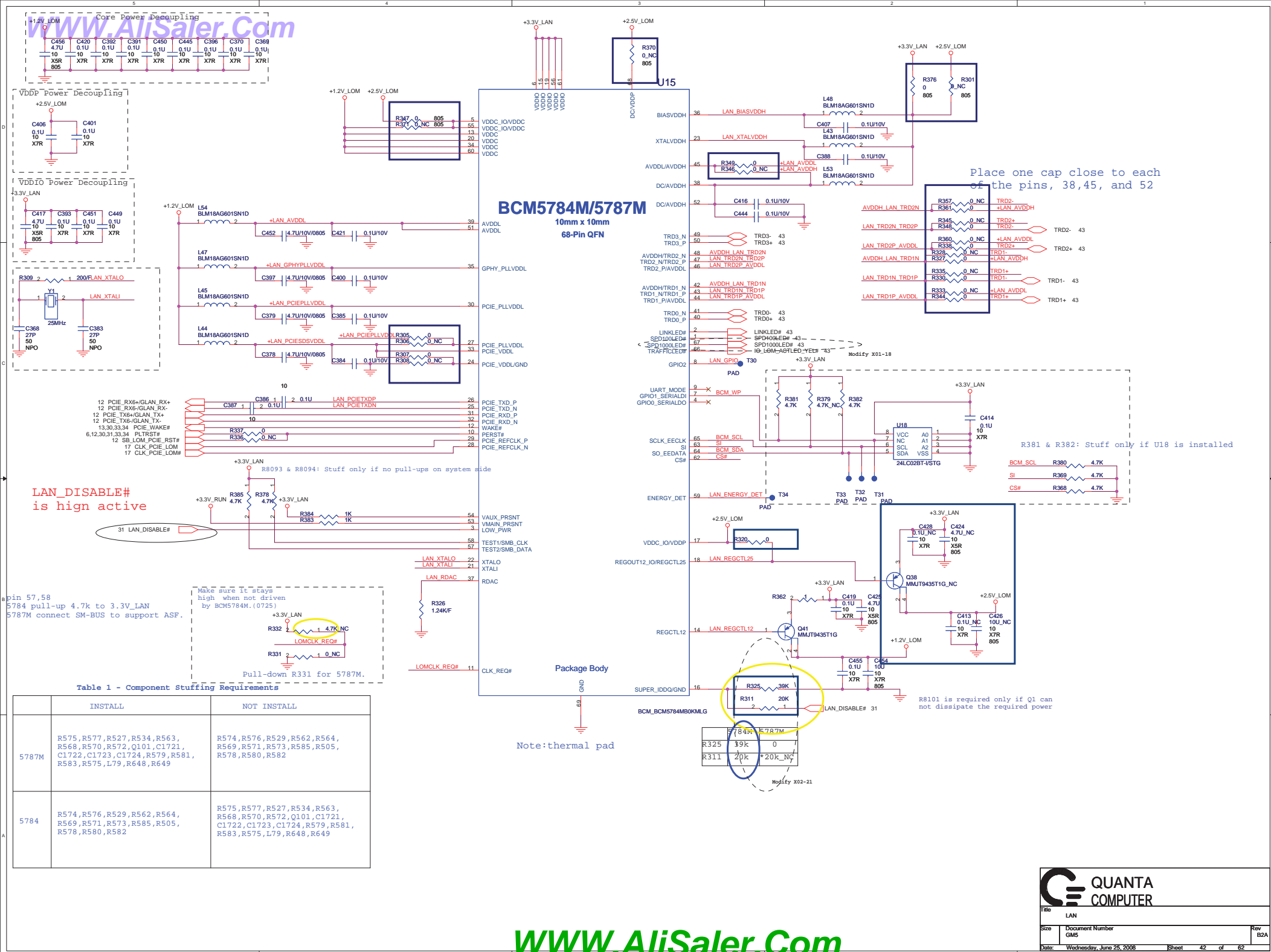




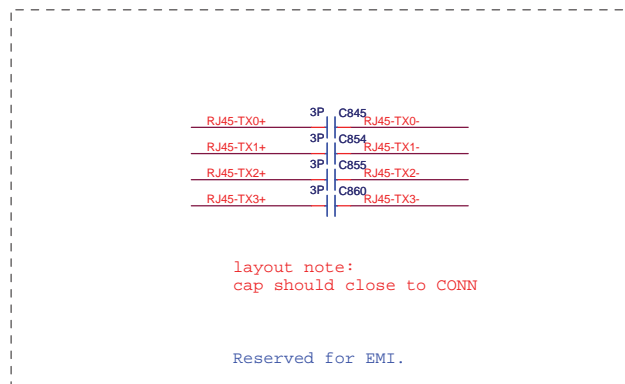
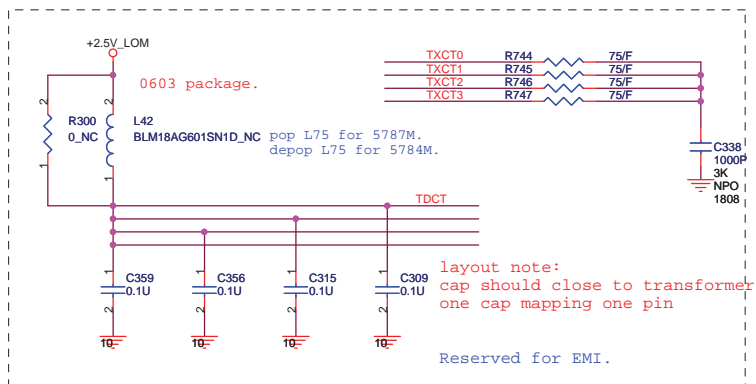
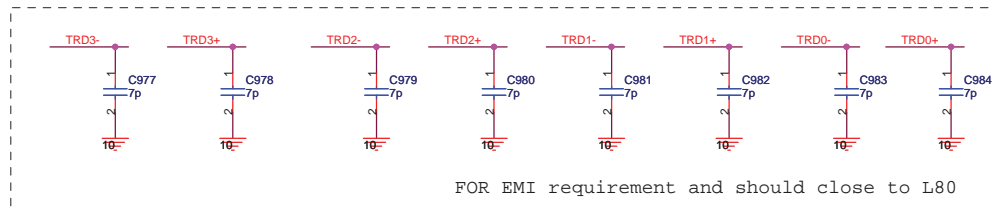
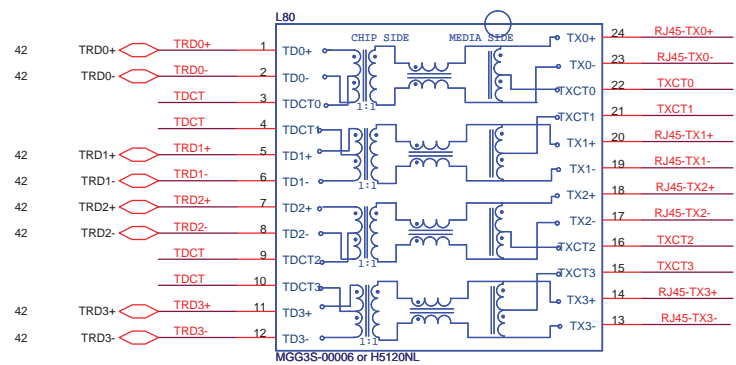
AUD FRONT L C519 1 2 0.01U 1206 LIN-  
 AUD FRONT R C518 1 2 0.01U 1206 RIN-  
 2.2U  
 AUD HP2 L0 C525 2 1 2.2K HP2 OU-  
 AUD HP2 R0 C524 2 1 2.2K HP2 OU-



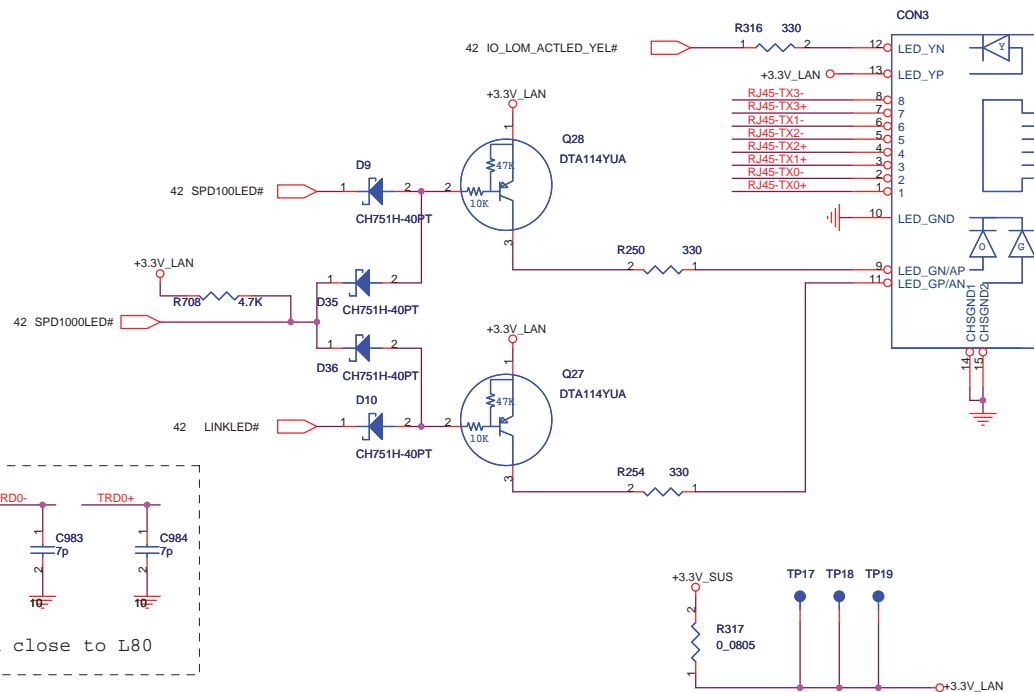


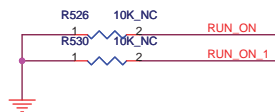
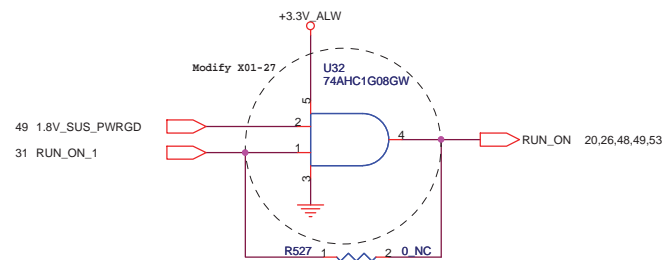
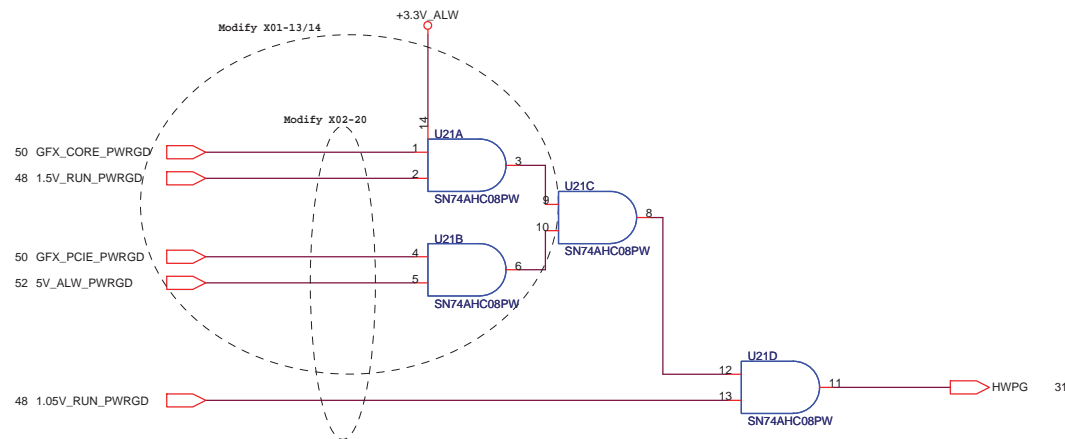
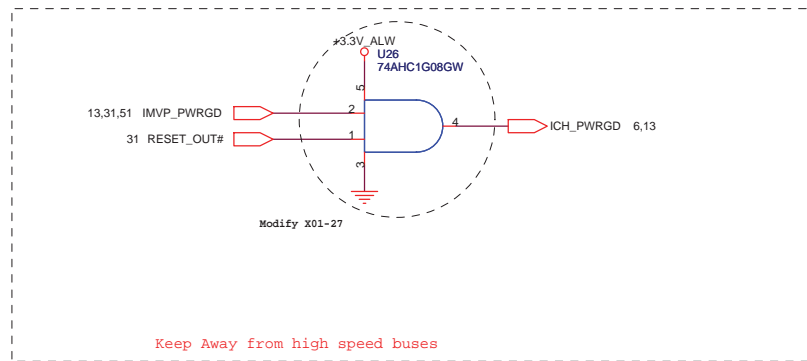


## TRANSFORM



## RJ-45 Connector




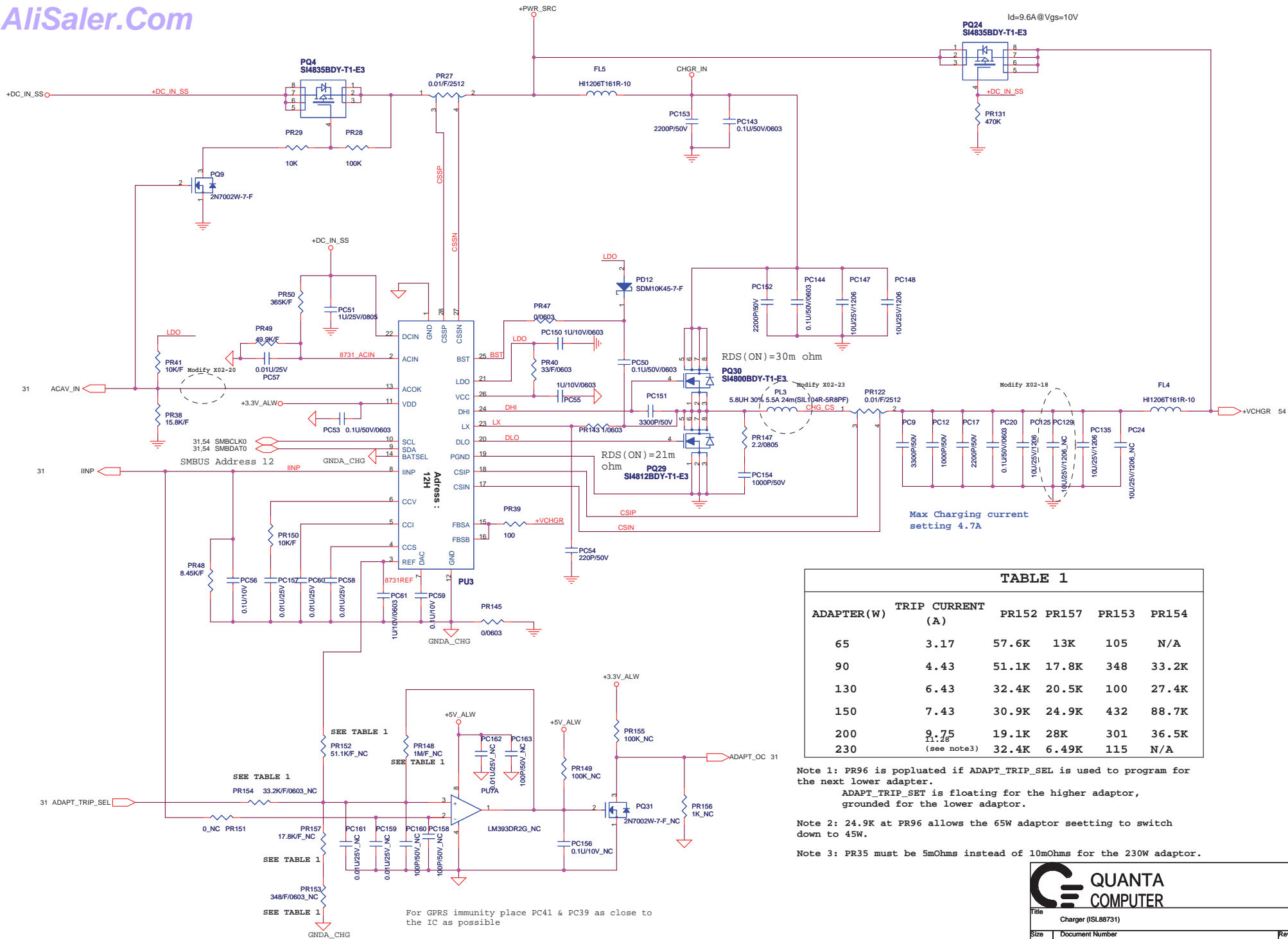


QUANTA COMPUTER			
Title System Reset Circuit			
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 <b>QUANTA COMPUTER</b>		
Title Battery Selector		
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Charger (SL88731)

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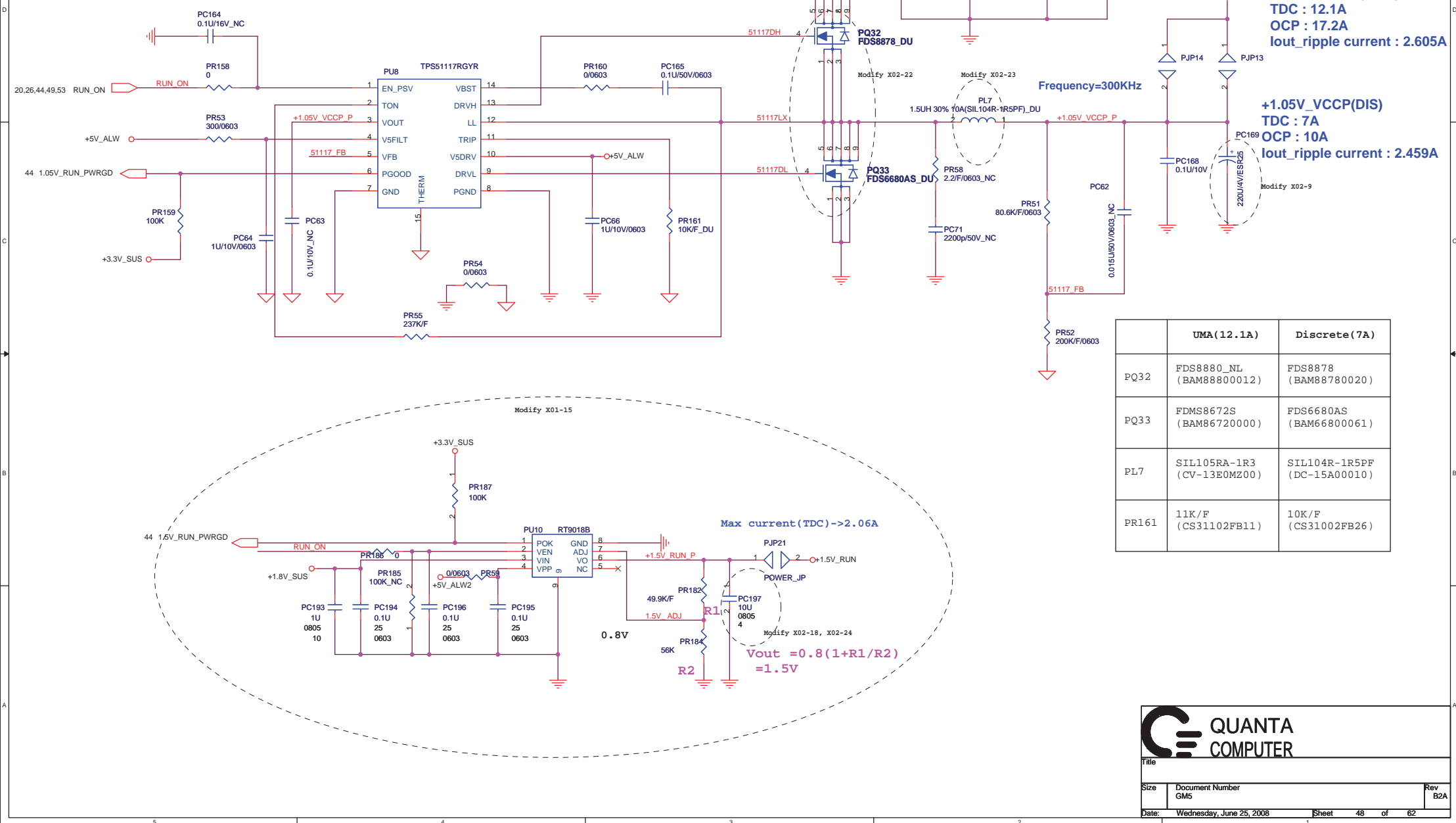
Title


Size

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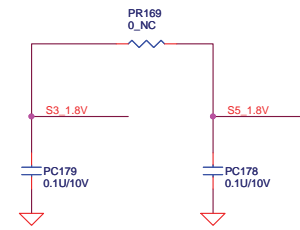
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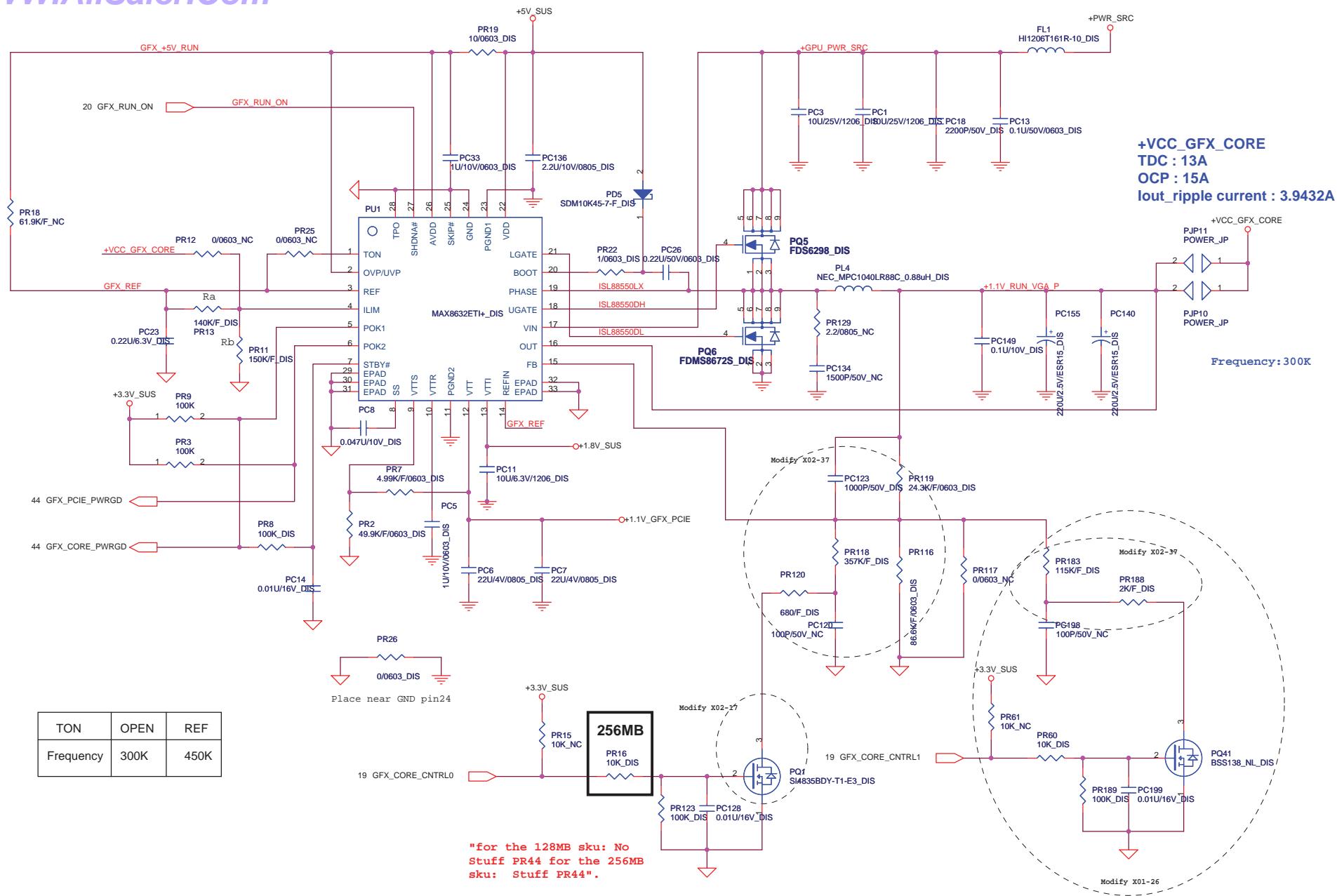


 <div> <div>QUANTA</div> <div>COMPUTER</div> </div>			
File 1.8VSUS & 0.9VTT (TPS51116)			
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**+1.8V\_SUS(UMA)**  
TDC : 10.25A  
OCP : 14.9A  
Iout\_ripple current : 4.868A





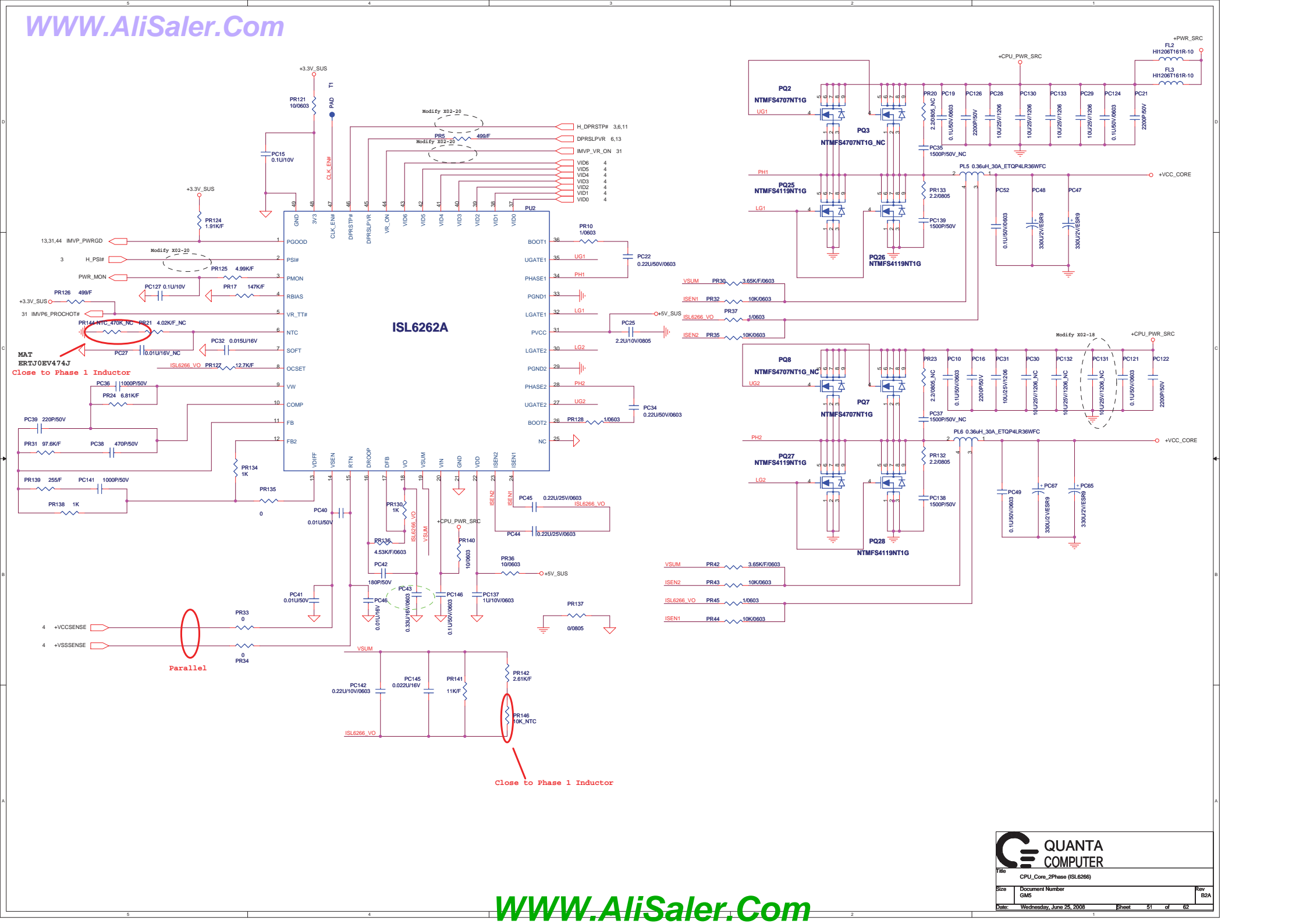
TON	OPEN	REF
Frequency	300K	450K

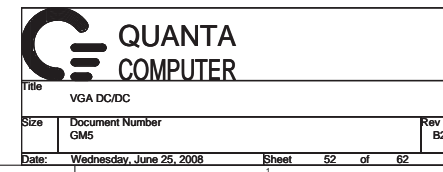
ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

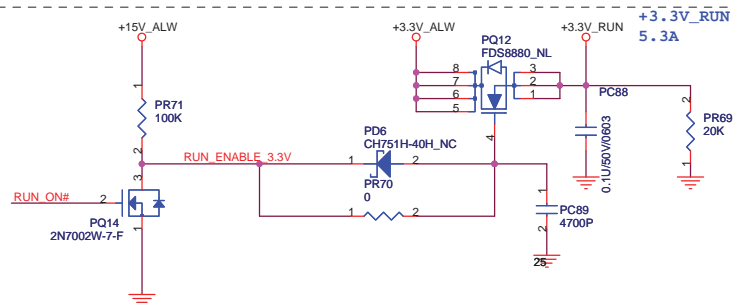
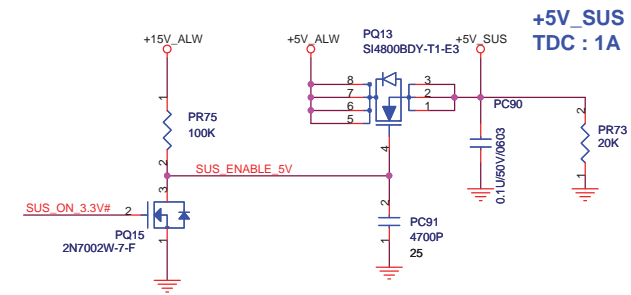
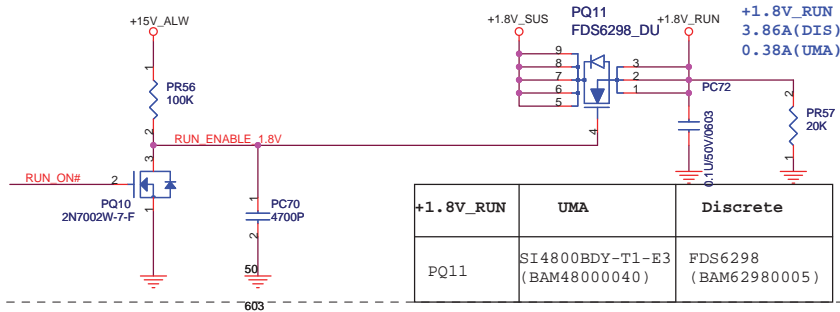
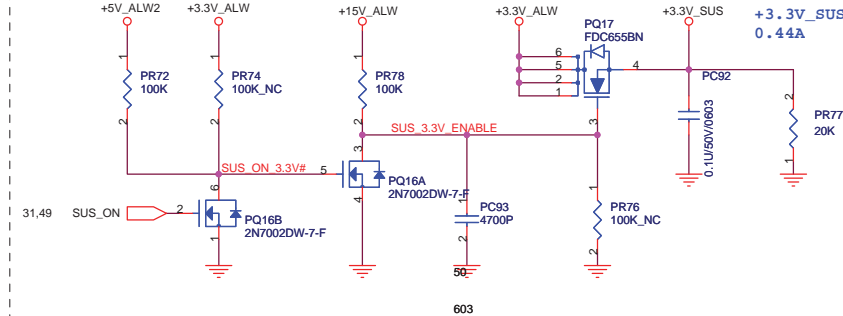
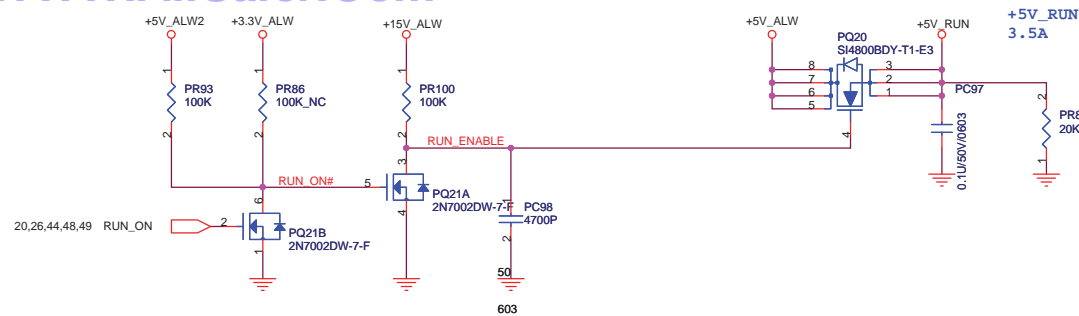
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.1V

Title: VGA DC/DC		
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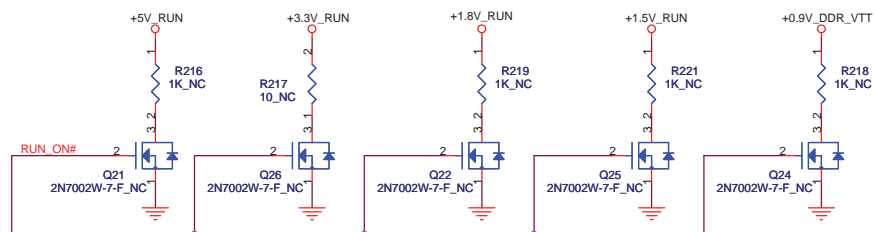




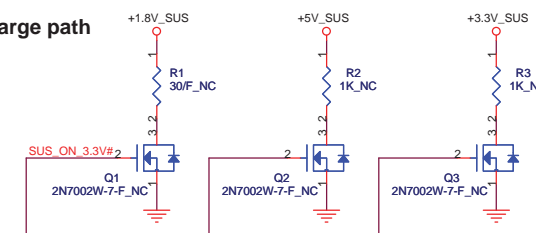




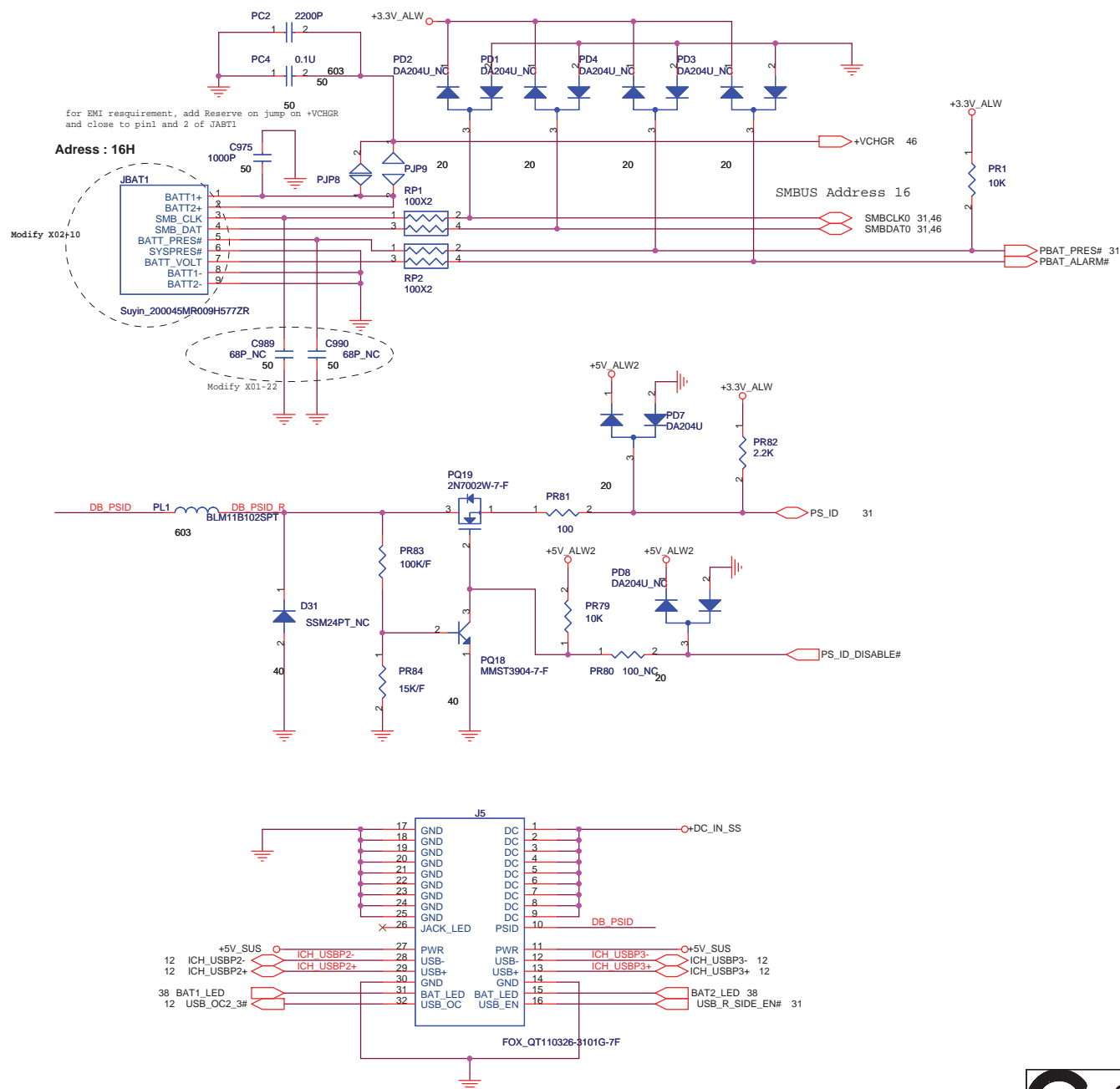
### Reserve discharge path



### Reserve discharge path



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Title DCIN,BATT CONNECTOR

Size

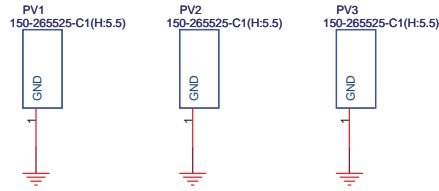
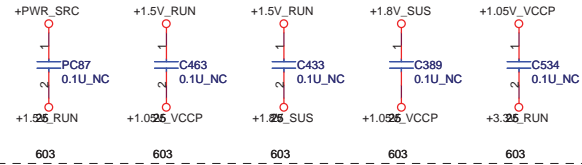
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Stitching caps



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SATA (HDD&CD\_ROM)

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PCCARD /CONN

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SIO(MEC5025)

Page 38  
Azelia CODEC

Page 40  
LAN(BCM5755M)

Page 48  
1.5VRUN,1.05V(VTT)

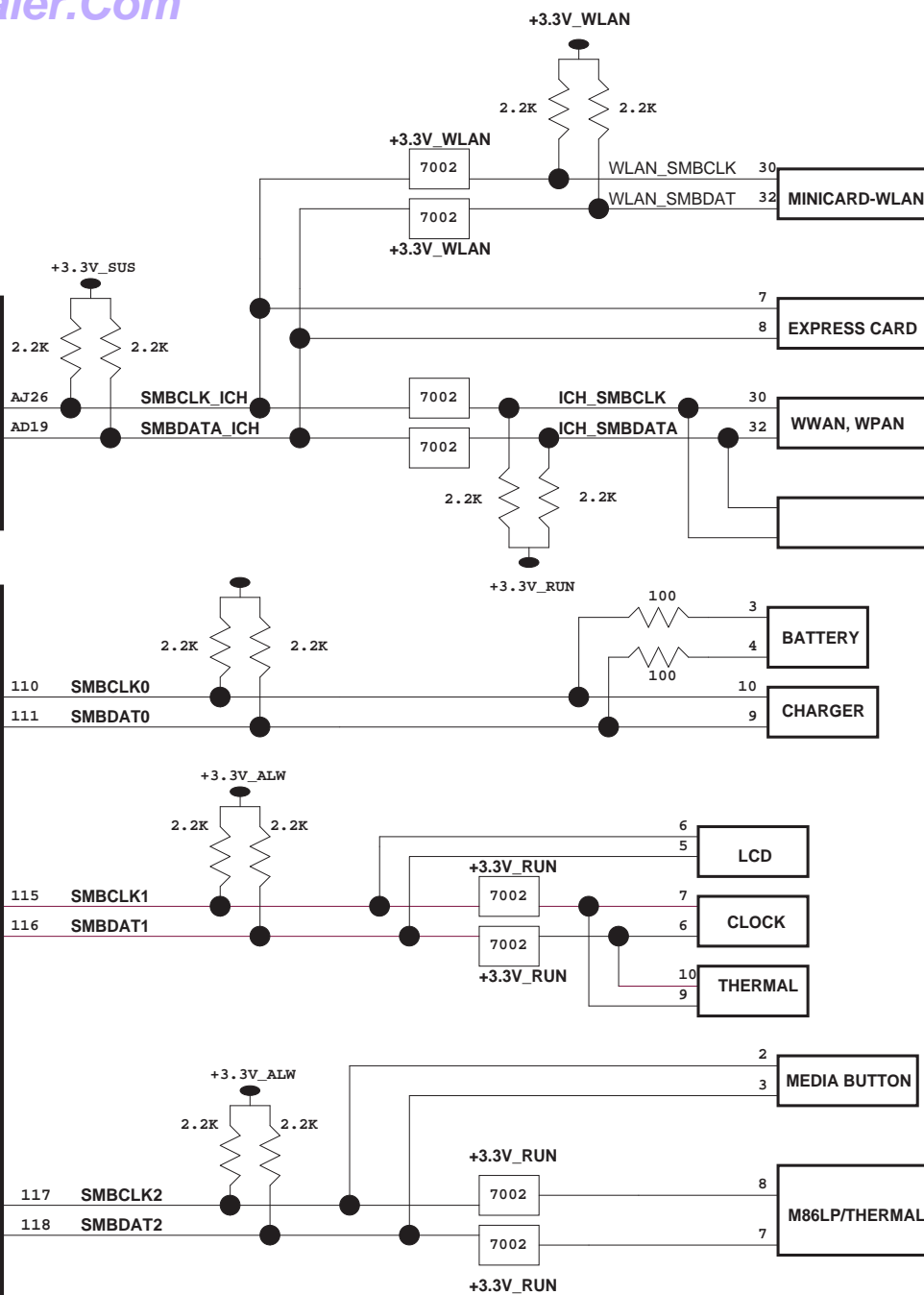
Page 49  
1.25V,1.8V,0.9V

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CPU\_MAX8786(3phase)

Page 52  
D/D Power

ICH9-M

SIO  
ITE8512





## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

## PM TABLE

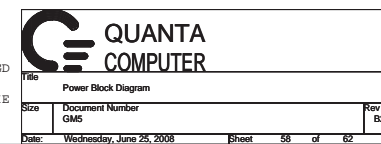
State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

## PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#0 / GNT#0	PIRQB: 1394 PIEQD: Card reader

ICH9-M	USB PORT#	DESTINATION
	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
ECE 5011	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None








Model	Rev	Page	Date	Rev	Description
Pacino MV of Intel	1	25	6/6 2008		Change JE4, L66, L70, L72 to DQCG990J00.
	2	43	6/6 2008		Change L80 to D86FXGLANG1.
	3	09	6/6 2008		Change D28 to BC01KAK5004.
	4	46	6/6 2008		Change PQ4, PQ24 to BAMA4835001.
	5	53	6/6 2008		Change PQ17 to BAMA4660102.
	6	25	6/11 2008		Reserve R9999, R10000, R10001, R10002, C4945, C4946, C4947, C4948 for EMI solution.
	7	6	6/11 2008		Change R187, R213 pull high to +3.3V_RUN to solve backdrive in S3.
	8	14	6/11 2008		Change C957 from CH2220KMJ1 to CH71001MB82
	9	48	6/11 2008		Change PC169 from CH733KM826 to CH722KMT800
	10	54	6/11 2008		Change JBA71 from DFH09MR013 to DFH09MR019
	11	11-14	6/11 2008		Change U48 from AJQP220T05 to AJQ0T100T01
	12	35	6/11 2008		Change JUSB1 from DFH04FR126 to DFH511FR016
	13	4,8,9	6/11 2008		Change C96, C188, C243, C438 to CH71001MB82
	14	40	6/11 2008		Change J3 from DFH04MR040 to DFWF04FR001
	15	38	6/11 2008		Change SW1 from DHLLS12P03 to DHLLS12P01
	16	35	6/11 2008		Change L17, L20, L50 from CX05Q2T1001 to DC0900A014
	17	50	6/11 2008		Change PQ1 from BAMA00350000 to BAMA48350024
	18	21,48, 46,49	6/11 2008		NC PC131, PC129, PC197, PC34 depended on internal notice.
	19	25	6/11 2008		Change U13 to UMA part.
	20		6/11 2008		Delete reserved 0-ohm resistors: R192, R139, R226, R144, R145, R161, R248, R197, R198, R198, R188, R173, R195, R177, R209, R174, R196, R178, R215, R201, R176, R200, R179, R202, R175, R199, R180, R153, R192, R154, R140, R195, R228, R857, R717, R716, R241, R220, R206, R209, R210, R212, R245, R546, R847, R140, R848, R730, R842, R815, R871, R776, R769, R718, R664, R847, R866, R663, R705, R701, R700, R694, R145, R142, R77, R81, R76, R162, R195, R804, R767, R768, R683, R437, R547, R576, R575, R579, R428, R424, R422, R420, R423, R646, RPR14, PR4, PR6, PR97
	21	42	6/12 2008		Change R325 to 39K-ohm and R311 to 20K-ohm for LAN chip, BCM5794M.
	22	48	6/12 2008		Change PQ32 & PQ33 subsystem ID to PWR.Plane.Regulator_1p05v1p0v.
	23	46, 48	6/12 2008		Change PL3 to CV-5855T204 & PL7 to DC-15A00002.
	24	48	6/12 2008		Populate PC187 by power's request.
	25	14	6/12 2008		Change U53 to DELL PSL LDO part and schematic.
	26	40	6/13 2009		Change Audio codec U91 to revision C1, AL79C1X0B03 for ST built.
	27	25	6/13 2009		For HDMI pre-amp item, DCCCEFC Capacitance, add low-Capacitance MOSs on SMBUS between HDMI connector and PIV(DPA111LS2DE.
	28		6/13 2009		Change C96, C98, C987, C438, C188, C243, C435, C595, C593, C957 to 220uF CAP2.0; CH722AM816.
	29	28	6/13 2009		Depopulate R819, because R5C833 don't need PME#.
	30	31	6/13 2009		Change the B0D to ST stage.
	31		6/13 2009		Change L87, L86, L91, L20, L17, L50, L46 to CXCG900U000.
	32	38	6/13 2009		Change SW1 to DHLLS12P03
	33	41, 52	6/13 2009		Delete reserved 0-ohm resistors R826 and PR92.
	34	52	6/13 2009		Reserve a CAP PC200 for girth reducing of TEMP_FAIL.
	35	33	6/17 2009		Change C655 to 100uF CAP, CH7101MB800.
	36	19, 52	6/18 2010		DELL's request on thermal detect pin
	37	50	6/19 2010		Change PR119 to CS32433P915(0603), PR116 to CS3862F90A(0603), PR118 to CS4837ZF910(0402), R120 to CS4168ZF910(0603), PR185 to CS4115ZF909(0402), PR188 to CS2002ZF901(0402) to meet GPU core voltage step: 0.9V, 0.95V and 1.1V.
	38	3,4	6/23 2009		Change CPU socket(L42) PIN to DGT*6000001(Foxconn)
	39	3	6/23 2009		NC R116 for H_RESET# glitch.
	40	25	6/24 2009		Fine-tune the emphasis and the equalization of HDMI. 1. Pull OC1, OC2 to high and Pull OC1, OC3 to low. 2. Pull EC1, 1 to low and pull EC1, 2 to high.
	41	15	6/24 2009		Change JDM1 to Hx5.6mm connector, DGMK0000015 and JDM2 to H=10.1mm connector, DGMK0000016.
	42	31	6/26 2009		NC R601, R704 and populate R593 for activating platform reset signal.



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E						
D						
C						
B						
A						



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